ISSCC 2021 Call for Papers

IEEE International Solid-State Circuits Conference

Sunday-Thursday, February 14-18, 2021

San Francisco Marriott Marquis, San Francisco, CA

ISSCC website: http://isscc.org

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The ISSCC 2021 Conference Theme is "Integrated Intelligence is the Future of Systems"

Circuits are no longer used simply as isolated functions, but rather part of an expanding world more complex, and all around us. Correspondingly, IC functions are becoming more sophisticated with a focus on building larger smart integrated systems. We still need some general work-horse components, such as, advanced accelerators, GHz to THz radios to communicate, sophisticated sensors, along with new ways to convert data from analog to digital. At the same time, power management is evolving to make systems more energy efficient. Specialized circuits are used to accelerate Artificial Intelligence algorithms to better understand the world. Furthermore, new packaging technologies will enable complex multi-chip systems, and emerging devices are expected together with new architectures and algorithms to enable new systems' functions, and ultimately future smart applications that are not yet envisioned.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; MEMS/sensor interface circuits.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; analog to information conversion; time-to-digital converters.

DIGITAL CIRCUITS, ARCHITECTURES & SYSTEMS*: Digital circuits, building blocks, and complete systems (monolithic, 2.5D, and 3D) for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video and multimedia, cryptography, smart cards, security and trusted computing, accelerators, reconfigurable systems, near- and sub-threshold systems, emerging applications. Digital circuits for intra-chip communication, clock distribution, soft-error and variation-tolerant design, power management (i.e. voltage regulators, adaptive digital circuits, digital sensors), PLLs for digital clocking applications, and security circuits (i.e. PUFs, TRNGs, side-channel attack countermeasures, and attack-detection sensors).

IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and SoCs; automotive, LIDAR, and ultrasonic sensors; MEMS sensor systems; wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; display electronics, displays with sensing functionality; sensing for AR/VR.

MACHINE LEARNING AND AI: Chips demonstrating system, architecture and circuit innovations for machine learning and artificial intelligence: processor architectures, accelerators and digital circuits; mixed-signal, analog, near-sensor and in-sensor processing schemes; all architectures and circuits leveraging near-memory and in-memory computation for AI using volatile or non-volatile memories. Hardware optimizations for new ML models including transformers, hyper-dimensional computing, spiking neural networks, etc.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, and fault tolerance; application-specific circuit enhancements within the memory subsystem, including in-memory logic functions and compute.

POWER MANAGEMENT: Power management and control circuits, regulators; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators; robust power management circuits for automotive and other harsh environments; circuits for lighting, wireless power and envelope modulators.

RF CIRCUITS and WIRELESS SYSTEMS:** Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs, and SiPs. Innovative circuit-level and system-architecture solutions for established wireless standards and future systems or applications such as radar, sensing, and imaging.

TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical, sensor interfaces, analog signal processing, power management, computation (including non-CMOS machine learning), data storage, and communication; non-silicon-, carbon-,organic-, metal-oxide-, compound-semiconductor- and new-device-based circuits; nano, flexible, large-area, stretchable, printable, spintronics, quantum, optical, integrated photonics, and 3D-integrated electronics.

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, equalization, robustness, adaptation capability, and design methodology; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

** This category will be reviewed by either the Digital Circuits or Digital Architecture/Systems subcommittee.*

*** This category will be reviewed by either the RF or Wireless subcommittee.*

Deadline for Electronic Submission of Papers:

Wednesday, September 9, 2020 • 3:00PM Eastern Daylight Time (19:00 GMT)

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STUDENT ACTIVITIES

Student-Research Preview (SRP): This session provides students with the opportunity to showcase the directions of their work, and to exchange experiences with other students and researchers from academia and industry. SRP is organized as an Evening Session consisting of short presentations of work-in-progress followed by a poster session. The abstract submission deadline for SRP is October 24, 2020. Refer to the ISSCC Website for more information.

Student Travel Grant Awards: Students who are members of the Solid-State Circuits Society and in a Ph.D. program can apply for partial travel support to attend ISSCC. Visit the SSCS website https://sscs.ieee.org/about/awards for more information.

Silkroad Award: The winner(s) are selected from first-time student-presenting authors at ISSCC whose research is conducted in an emerging region in the Far East.

DEMONSTRATION SESSIONS:

Authors of regular papers are eligible for consideration for Demonstration Sessions. The demonstrations will be held during the Conference social hours on Monday and Tuesday. At these sessions, authors of selected papers will employ posters to augment their demonstration. To be considered for participation in the Demonstration Sessions, authors, during the submission process, must communicate their intention to provide a demo. Refer to the ISSCC Website for further information (http://isscc.org).

ELECTRONIC SUBMISSION OF ABSTRACT, DRAFT MANUSCRIPT, AND PRE-PUBLICATION MATERIAL:

Authors should submit 2 items for review: 1) An informative and quantitative **Abstract**; 2) A **Draft Manuscript** including figures for the Digest of Technical Papers. Be sure to read the Pre-Publication Guidelines (summarized below) carefully.

The Submissions Website will be available starting July 1, 2020. You may consult the Website for instructions at any time after this date. To submit a paper, go to: https://submissions.mirasmart.com/ISSCC2021 to upload the manuscript and provide the requested additional information. Abstract and manuscript must be submitted by September 9, 2020. During the submission process you will be asked for a suggested subject area, however this subject area may be changed by the ISSCC organization to streamline the review process. A sample abstract and draft Digest paper can be found at the ISSCC Website (single-column double-spaced format is required for the paper-review process). All speakers will have the possibility to present their paper remotely, if requested.

ADDITIONAL SUBMISSION DETAILS:

The **Abstract** must be uploaded to the **Submissions Website**. It must not exceed 500 characters (including spaces). The Abstract must be factual and provide as complete and quantitative a description as possible, including specific and concrete performance data. Claims such as “new”, “advanced”, “novel”, “high-performance”, and “high-speed” are not acceptable. Please refer to the sample abstract on the ISSCC Website. Note that ISSCC reserves the right to modify the paper title and abstract when technically appropriate.

Three PDFs must be uploaded to the Submissions Website, as defined by the ISSCC templates: The first, for the draft manuscript text, is limited to 4 pages in single-column double-spaced format, using 12 pt Arial Narrow font with fewer than 8,700 characters (including spaces, title, and 3 to 6 references. The second, for the figures, must not exceed 10 pages with one figure including caption per page. The first 7 figures, including a die photo must be referred to in the text. In addition, up to 3 optional supplementary figures can be included for review purposes. We strongly encourage you to include a comparison table as one of the figures. The manuscript text must contain all essential information, including relevant references. Papers exceeding the length limit will be immediately rejected, as requiring length editing. Complex multipart figures are not allowed (for example,

Figures 2a and 2b will be counted as two figures!). Tables count, and are labeled, as figures. If a die-photo and/or comparison table is available, they can be included as part of the 7-figure limit. Supplementary figures will **NOT** be part of the final manuscript, and should **NOT** be referred to in the text of the paper, but serve ONLY as additional material for the reviewers. These 3 figures should be described with no more than 4 sentences in their captions with figures labeled as "Fig. S1, S2, S3". The third, for additional references. For further details, see the ISSCC Website.

Double-Blind Review. The paper selection will follow a double-blind review process, meaning that both the authors and reviewers will remain anonymous during the paper selection process. All authors **MUST** adhere to the following guidelines to conceal their identity: (1) Eliminate names, contact information, and affiliations from the entire manuscript (including **PDF metadata, logos on die photos, logos on printed circuit board photos,** etc.). (2) Cite all relevant prior work (**including your own**) in the third person (for example, "It has been shown that… [1]"; do not use the words "my" or "our"). Work that is substantially related to the submission and has been submitted to another Conference/Journal, but has not been published yet, **must be cited in an anonymized format*** and **must be uploaded as supplementary material**. Supplementary material does not need to be anonymous, as it will be checked only after paper selection. Do not cite patents. (3) Eliminate acknowledgments and references to funding sources. (4) Do not contact the program committee members to solicit input on your manuscript. The identity of authors is only known to the program chair/vice-chair and the subcommittee chairs; you may contact them for questions. Manuscripts that are not properly anonymized cannot be considered for review; to ensure your submission complies with these rules please review carefully the sample manuscript, the FAQ on Double-Blind Review, and the guidelines on how to write a good submission at the ISSCC Website. The review process will include a software-based plagiarism check. After paper selection, a final pre-publication check (using the authors' names) is applied using the guidelines summarized below. ISSCC may withdraw any paper that violates the pre-publication guidelines.

The most common reason for paper rejection is a lack of clear evidence of what is novel in the work, and the extent to which it advances the state-of-the-art. Successful submissions contain specific new results, sufficient detail and data to be understood technically, circuit schematics, measured results for key elements, and tabulated comparisons with recently-published work, where appropriate.
For further details on manuscript preparation, check the ISSCC Website: http://isscc.org, or send an email with your questions to the Director of Publications: Laura Fujino, Email: lcfujino@aol.com. All information regarding submission is also available at the Submissions Website (https://submissions.mirasmart.com/ISSCC2021).

Notification of Acceptance: Authors will be notified of acceptance by October 19, 2020. A submission may be accepted as either a regular or short paper. A regular paper is allowed 30 minutes (23 minutes presentation time). A short paper is allowed 15 minutes (12 minutes presentation time). Regular and short papers must meet the same submission and quality standards. They differ only in the determination by the Program Committee of the time required to present their key ideas.

Authors of accepted papers will have an opportunity to modify their manuscript. All information removed/anonymized following the Double-Blind Review guidelines (logo on-die photo, etc.) may be added back to the final paper upon acceptance. The Program Committee may require specific additional revisions. There will be further formatting requirements for the final Digest manuscript. The presenting author is required to register for the Conference in advance.

*Citation in anonymized format: [1] Details withheld in accordance with double-blind review process (paper attached as supplementary document).

The Conference Pre-Publication Policy: As the premier global forum for the debut of technical innovations in integrated circuits and systems, ISSCC cannot accept papers whose key innovative ideas and results have already been disclosed to the public. To assess the novelty of a paper, the program committee evaluates its content against all background or baseline information that was pre-published by the authors. Disclosures considered as pre-publication include: (1) Publicly available data in articles, manuals, data sheets, trade journals, application notes, other conferences, and press releases, which contain substantial technical information such as schematics, principles of operation, architectures, and algorithms. (2) Some previously publicly copyrighted material, such as in an IEEE publication. (3) Material submitted for which publication decision is still pending. (4) Material accepted for publication elsewhere. (5) Material available on a public website at any time up to the first day of the next ISSCC. Disclosures **not** considered pre-publication include: (1) Electronic copies of articles posted by authors on publicly accessible websites or preprint servers such as arXiv.org. IEEE policy regarding sharing and posting of articles is described in the IEEE Author Center. (2) Preliminary datasheets or a product announcement with no technical details. (3) Presentation at a limited-attendance workshop with no proceedings. A key element here involves the ability to find any handouts via electronic means or in a printed catalog. For example, if handouts are available to attendees of a workshop, but are not subsequently downloadable or orderable, this is acceptable. (4) Information from an advance program or information from IEEE-sponsored press meetings after publication or formal press release. (5) Information provided under non-disclosure agreements (NDA) to customers, partners, or other parties, (6) Final, signed versions of Master's or Ph.D. theses available in open repositories, either printed or online. A thesis published for profit is an exception, and is considered prepublication. (7) Published patents and patent applications. Authors must disclose all material that may fall into the pre-publication category as part of the submission process.

For further details on Pre-Publication Policy, Double-Blind Review or assistance in assigning a subject area, contact the Program Chair:
Makoto Ikeda, Tel: +81 90-5759-6065, Email: ikeda@silicon.u-tokyo.ac.jp

POLICY REGARDING PAPER-SUBMISSION DEADLINE

Due to the timing constraints associated with the paper review process, Paper Submissions must be received by the deadlines shown below to be considered by the Program Committee.

DEADLINE FOR ELECTRONIC SUBMISSION OF PAPERS:

Wednesday, September 9, 2020 • 3:00 PM Eastern Daylight Time (19:00 GMT)

ISSCC 2021

SUNDAY-THURSDAY — FEBRUARY 14-18, 2021

SAN FRANCISCO MARRIOTT MARQUIS HOTEL, SAN FRANCISCO, CA

Deadline for Electronic Submission of Papers:
Wednesday, September 9, 2020 • 3:00PM Eastern Daylight Time (19:00 GMT)

Given the on-going Covid-19 pandemic, there is currently uncertainty in the format of the Conference. However, the safety of our speakers and attendees will remain of paramount concern. Thus, we will be fully prepared to deliver a virtual conference that will continue to preserve the high-quality and rich-experience characteristic of ISSCC. Please check the ISSCC website for updates.

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PLEASE CIRCULATE/POST ON BULLETIN BOARDS

SAN FRANCISCO MARRIOTT MARQUIS, SAN FRANCISCO, CA / FEBRUARY 14-18, 2021

IF YOU NEED TECHNICAL ASSISTANCE, PLEASE CONTACT THE APPROPRIATE SUBCOMMITTEE CHAIR OR REGIONAL SECRETARY

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