IEEE SOLID-STATE CIRCUITS SOCIETY

2020 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE
FEBRUARY 16, 17, 18, 19, 20
CONFERENCE THEME: INTEGRATED CIRCUITS POWERING THE AI ERA
SAN FRANCISCO MARriott MARQUIS HOTEL

5-DAY PROGRAM

THURSDAY ALL-DAY
4 FORUMS: ML PROCESSORS; ELECTRICAL/OPTICAL TRANSCIEVERS; POWER MANAGEMENT FOR FUTURE SOCs; SENSORS FOR HEALTH
SHORT-COURSE: CIRCUIT DESIGN IN ADVANCED CMOS

SUNDAY ALL-DAY
2 FORUMS: mm-Wave 5G; ML as Killer App
10 TUTORIALS: INTEGRATED TRANSFORMERS; DCDC CONVERTERS; WEARABLE/IMPLANTABLE SENSING; NONVOLATILE MEMORIES (MRAM, RRAM, PRAM); TIME-INTERLEAVED ADCS; DIGITAL FRACTIONAL-N PHASED LOCKED LOOP; LOW-DROPOUT INTEGRATED REGULATORS; CAPACITIVE SENSOR INTERFACES; WIRELESS TRANSCIEVER CIRCUITS/ARCHITECTURES (2G TO 5G); UNDERSTAND/EVALUATE DL PROCESSORS
2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; RISING STARS 2020

NEW THIS YEAR!
HIGHLIGHTED CHIP RELEASES
ISSCC VISION STATEMENT
The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS
On Sunday, February 16th, the day before the official opening of the Conference, ISSCC 2020 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A WiC Workshop on “Rising Stars 2020” will be offered starting at 4:00 pm. In addition, the Student-Research Preview, featuring ??? ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Tadahiro Kuroda, Professor, University of Tokyo.

On Monday, February 17th, ISSCC 2020 at 8:30 am offers four plenary papers on the theme: “Integrated Circuits Powering the AI ERA ”. On Monday at 1:30 pm, there begin five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. On Monday evening there is one event. At 8:00 pm “Industry Showcase” will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation.

On Tuesday, February 18th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled “Quiz Show: “The Smartest Designer in the Universe” and “Open-Source Hardware Revolution”.

On Wednesday, February 19th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 20th, ISSCC offers a choice of five all-day events:

- A Short Course entitled: “Circuit Design in Advanced CMOS Technologies — Considerations and Solutions ”
- Four Advanced-Circuit-Design Forums entitled:
  - “Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking”
  - “Cutting Edge Advances in Electrical and Optical Transceiver Technologies”
  - “Power Management as an Enabler of Future SoCs”
  - “Sensors for Health”

This year, again, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.
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There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

**Ali Sheikholeslami**  
ISSCC Education Chair

**8:30 AM**

**T1: Fundamentals of Integrated Transformers:**  
*From Principles to Applications*  
*Andrea Bevilacqua, University of Padova, Padova, Italy*

Integrated magnetic transformers are becoming ubiquitous in mm-wave and RF systems, while also finding application in fully integrated DC-DC converters. This tutorial will cover the fundamentals of transformer operation spanning from the underlying physical principles, to the link between the magnetic parameters (inductances and magnetic coupling) and the inductor geometry, to its use in the design of building blocks like LNAs, PAs, VCOs, etc. The advantages and possibilities of using a transformer for the implementation of baluns, impedance transformation networks, higher-order resonant networks, feedback circuits, etc. will be highlighted.

**Andrea Bevilacqua** received the Laurea and Ph.D. degrees in Electronics Engineering from the University of Padova, Italy. From 2005 to 2015, he was Assistant Professor with the University of Padova, where he is now Associate Professor. His current research interests include the design of analog and RF/microwave integrated circuits and the analysis of wireless communication systems, radars, and DC-DC converters. He is author or coauthor of more than 90 technical papers, and he holds 5 patents. He serves on the ISSCC and ESSCIRC Technical Program Committees and was TPC Co-Chair of ESSCIRC 2014.

**8:30 AM**

**T2: Analog Building Blocks of DC-DC Converters**  
*Bernhard Wicht, University of Hannover, Hannover, Germany*

System behavior and performance of power management strongly depend on the implementation at the circuit level. This tutorial covers the design of DC-DC converter building blocks such as power switches, gate drivers and their supply, level shifters and error amplifiers, as well as control-loop and current-sensing techniques. Circuits for diagnostics and protection will also be addressed. Increasing switching frequency scales down passive components, but poses a challenge for the design of timing-critical circuits. The tutorial will highlight trade-offs between speed, efficiency, complexity, voltage and current capabilities, etc.

**Bernhard Wicht** has 20+ years of experience in analog and power-management IC design. He received the Dipl. Ing. degree in electrical engineering from TU Dresden, Germany, in 1996 and the Ph.D. degree from TU Munich, Germany, in 2002. Between 2003 and 2010, he was with Texas Instruments, Germany, responsible for the design of automotive ICs for power management, motor control and transceivers. Between 2010 and 2017, he was a full professor and a member of the Robert Bosch Center for Power Electronics at Reutlingen University. Since April 2017, he has been heading the Chair for Mixed-Signal IC Design at Leibniz University Hannover, Germany.
Wearable and implantable systems offer an exciting means to monitor human physiology in real time. Such devices require careful interaction between transducers and front-end circuits in order to extract the maximum possible signal-to-noise ratio, while also carefully managing system-level size and power trade-offs. This tutorial will introduce front-end design techniques used in electrophysiological sensing applications, along with emerging trends in physiochemical sensing applications.

Patrick Mercier is an Associate Professor of Electrical and Computer Engineering and co-founder/co-director of the Center for Wearable Sensors at UC San Diego. He received his B.Sc. degree from the University of Alberta, and the S.M. and Ph.D. degrees from MIT. His research interests include the design of energy-efficient mixed-signal systems, RF circuits, power converters, and sensor interfaces for wearable, medical, and mobile applications. This has led to over 120 peer-reviewed papers. He has received numerous awards, including the DARPA Young Faculty Award, the NSF CAREER Award, and the 2010 ISSCC Jack Kilby Award. He is an Associate Editor of TBioCAS and SSCL, and is a member of the ISSCC, CICC, and VLSI technical program committees.

NAND Flash and eFlash have been the workhorse of memory hierarchy for standalone storage and embedded non-volatile memories (NVMs), respectively. But with the ever-increasing need for memory capacity and bandwidth, due to new applications in graphics, AI and IoT, device and circuit designers have been heavily investigating alternative memories to fill the need. When it comes storage, there is a big gap between DRAM and NAND in terms of density and speed, which could justify a new memory type. When it comes to NVM, growing IoT requires better performance and more power-efficient NVM than eFlash, which can be scaled to 1xn techologies.

This tutorial will talk about the basic characteristics, circuits and system designs for emerging non-volatile memories such as MRAM, RRAM, and PRAM. The tutorial will present the details of MRAM and RRAM, as well as a comparison of these memory devices, and the applications they target.

After finishing the Ph.D. in EE at the University of Virginia in 2002, Fatih joined Logic Tech. Development at Intel. Since then, he has been working on memory developments, such as SRAM, DRAM, MRAM and RRAM. He has served as technical committee member at VLSI Symp. Circuits and ISSCC. He has co-authored more than 40 papers and he’s co-inventor of more than 30 patents.
10:30 AM

T5: Fundamentals of Time-Interleaved ADCs  
John P. Keane, Keysight Technologies, Santa Clara, CA

In recent years, time-interleaving analog-to-digital converters (ADCs) have become more popular, especially for high sample rate applications such as wireline communications. This tutorial will cover the fundamentals of time-interleaved sampling, including an introduction to aliasing and an explanation of how mismatch in time-interleaved architectures can cause aliasing artifacts to appear. Practical methods to implement time-interleaved ADCs and combat these mismatch-induced effects will also be presented.

John P. Keane received the Ph.D. degree in Electrical Engineering from the University of California, Davis in 2004. Since then, he has been with Keysight Technologies (formerly Agilent Technologies), Santa Clara, CA, where he is engaged in research on high-performance integrated circuits for measurement applications. His research interests include timing recovery and adaptive equalization for high-speed serial transceivers and the design and calibration of high-resolution data converters. Most recently his focus has been on the design of high-bandwidth time-interleaved analog-to-digital converters. He is a co-author of several IEEE papers and US patents on these topics and is currently a member of the ISSCC technical program committee.

10:30 AM

T6: Digital Fractional-N Phase-Locked-Loop Design  
Mike Shuo-Wei Chen, University of Southern California, Los Angeles, CA

The tutorial overviews the basics of digital fractional-N phase-locked-loop architectures and their design principles from the signal-processing level down to circuit design. We will examine various design constraints and implementation overhead of such architectures due to the inherent digital architecture as well as circuit non-idealities. We will discuss circuit design and calibration techniques. Lastly, some real design examples in silicon with measurement data will be provided.

Mike Shuo-Wei Chen is Associate Professor in the Electrical Engineering Department at the University of Southern California (USC) and holds Colleen and Roberto Padovani Early Career Chair position.

He received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1998 and the M.S. and Ph.D. degree from University of California, Berkeley, in 2002 and 2006, all in Electrical Engineering. As a graduate student researcher, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted today for low-power high-speed analog-to-digital conversion products in industry. At USC, he leads an analog mixed-signal circuit group. He was the recipient of NSF Faculty Early Career Development (CAREER) Award, DARPA Young Faculty Award (YFA) both in 2014.
Systems-on-chips incorporate integrated low-dropout (LDO) voltage regulators (VRs) to improve energy efficiency by allowing each core on a shared input voltage rail to operate at a unique voltage. LDOs enable compact size, low cost, and relatively simple integration. This tutorial introduces the key trade-offs between analog and digital LDOs and covers the primary specifications. Finally, this tutorial presents a wide range of state-of-the-art digital LDOs while highlighting the key design trade-offs.

Mingoo Seok is Associate Professor of Electrical Engineering at Columbia University. He received the B.S. degree with summa cum laude from Seoul National University, South Korea, in 2005, and the M.S. and Ph.D. degrees from the University of Michigan in 2007 and 2011 respectively, all in electrical engineering. His research interest is VLSI hardware, including near-threshold and subthreshold-voltage ultra-low-power hardware, machine-learning hardware, variation-tolerant hardware, on-chip power management, and non-conventional computing such as in-memory computing and hybrid analog-digital computing. He won the 2015 NSF CAREER award. He has been a technical committee member in hardware conferences including the IEEE International Solid-State Circuits Conference (ISSCC).

Capacitive sensors for displacement, proximity and pressure sensing are widely deployed in various consumer, medical, automotive, and industrial sectors, with the advantages of zero static power consumption and good compatibility with CMOS circuitry. This tutorial provides an overview of the fundamental principles of capacitive sensor interfaces, as well as the design tradeoffs in terms of accuracy and energy consumption. Recent techniques to achieve low-noise and high-efficiency sensing will also be discussed.

Man-Kay Law received the B.Sc. degree in Computer Engineering and the Ph.D. degree in Electronic and Computer Engineering from Hong Kong University of Science and Technology. Since 2011, he has been with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, where he is currently an Associate Professor. His research interests include ultra-low-power sensing circuits and systems, analog and mixed-signal integrated circuits, and energy harvesting techniques. He is a co-recipient of the A-SSCC Distinguished Design Award in 2015, and also the advisor for student awards, including the SSCS Pre-doctoral Achievement Award and the ISSCC Silk-Road Award. He is a member of the Technical Program Committee of ISSCC.
Cellular technology has witnessed five generations of evolution - the mobile UE-era ushered in by 2G (GSM/EDGE), to the future smart-phones that will powered by the enhanced spectral efficiency of 5G. Each ‘G’ improved the user experience while introducing new hardware design challenges. This tutorial follows a top-down approach - we compare 2/3/4/5G system requirements, derive key TX/RX/LO circuit specifications, and highlight the differences in circuit topologies suited for these contrasting specifications. Using this framework, circuit techniques to handle a diverse range of problems such as low phase-noise oscillators, improved blocker tolerance, single-RB linearity, and digital calibration will be introduced.

Venumadhav Bhagavatula received the B.E. degree in electronics and communication from the University of Delhi, New Delhi, India, the M.Tech. degree in electronic design technology from the Indian Institute of Science, Bangalore, India, and the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2005, 2007, and 2013. Since 2014 he has been with the Advanced Circuit Design group at Samsung Semiconductors Inc., San Jose, CA, USA. His research interests include RF/mm-wave and low-power mixed signal circuits. He currently serves on the technical program committee member for the ISSCC.

Vivienne Sze is an Associate Professor in the EECS Department at MIT. Her research interests include energy-aware signal processing algorithms, and low-power circuit and system design for applications, such as machine learning, computer vision, autonomous navigation, and video coding. Prior to joining MIT, she was a Member of Technical Staff in the R&D Center at Texas Instruments, where she developed algorithms and hardware for the H.265/HEVC video coding standard, which received the Primetime Engineering Emmy Award. She is a recipient/co-recipient of several awards including the Symposium on VLSI Circuits Best Student Paper Award, the MICRO Top Picks Award, and MIT’s Jin-Au Kong Outstanding Doctoral Thesis Prize.
Millimeter-wave frequencies have emerged as a promising solution to achieve increased wireless capacity and speed in 5G networks. The forum brings together experts who will describe challenges and state-of-the-art in circuits and architectures for 28GHz/38GHz 5G NR transceivers targeting UE, CPE and infrastructure applications. System-level deployment objectives and real-world constraints will be presented to provide the context for mm-wave transceiver designs. Different device technologies will be considered and system-level requirements will be translated to design approaches for critical building blocks for frequency synthesis, power amplification, RF-PA power supply systems and analog-to-digital conversion. Packaging and test considerations play an integral role in mm-wave transceiver design due to the high operating frequency and large number of elements. Low-cost mm-wave antenna and packaging will be presented along with phased array calibration and test approaches for a holistic overview of future mm-wave 5G landscapes.

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F2: ML at the Extreme Edge: Machine Learning as the Killer IoT App

Organizer: Dennis Sylvester, University of Michigan, Ann Arbor, MI

Committee: Meng-Fan (Marvin) Chang, National Tsing Hua University, Hsinchu, Taiwan
James Myers, Arm, Cambridge, United Kingdom
Naveen Verma, Princeton University, Princeton, NJ

This forum puts a clear focus on machine learning in very low power edge devices (uW to mW), rather than focusing on its use in data centers. While GPUs for training in data centers, and large-scale inference engines are the common case today, the combination of IoT and ML brings new capabilities to edge devices. Speakers will motivate this area and provide insights on the impact of resource constraints on both training and inference in such devices. In addition, key application areas are discussed in depth, namely audio and imaging. The role of new memory-centric design approaches in edge-based ML is also discussed. Finally, the software environment is discussed, to make hardware designers aware of the opportunities for power-constrained ML algorithm implementations.

**Agenda**

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<td>8:00 AM</td>
<td>Breakfast</td>
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<tr>
<td>8:20 AM</td>
<td>Introduction</td>
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<td></td>
<td>Dennis Sylvester, University of Michigan, Ann Arbor, MI</td>
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<td>8:25 AM</td>
<td>Machine Learning Meets IoT:</td>
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<td></td>
<td>The Perfect Storm for Innovation in Ultra-Low Power System Design</td>
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<td>Boris Murmann, Stanford University, Stanford, CA</td>
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<td>8:50 AM</td>
<td>TinyML: Ultra-Low Power Edge AI for Autonomous Systems</td>
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<td>Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA</td>
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<tr>
<td>9:40 AM</td>
<td>Bringing Intelligence to Mobile Platforms:</td>
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<td></td>
<td>From Deep Learning to Neuromorphic Computing</td>
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<td>Dongsuk Jeon, Seoul National University, Seoul, Korea</td>
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<tr>
<td>10:30 AM</td>
<td>Break</td>
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<td>10:45 AM</td>
<td>Structured Sparsity and Low-Precision Quantization for Energy-/Area-Efficient DNNs</td>
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<td>Jae-sun Seo, Arizona State University, Tempe, AZ</td>
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<td>11:35 AM</td>
<td>TinyML for Audio-Based Applications</td>
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<td>Shih-Chii Liu, University of Zurich and ETH Zurich, Switzerland</td>
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<td>12:25 PM</td>
<td>Lunch</td>
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<td>1:25 PM</td>
<td>Machine Learning for Event-Based Vision:</td>
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<td>from Low Power Pixels to Low Power Applications</td>
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<td>Amos Sironi, Prophesee, Paris, France</td>
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<td>2:15 PM</td>
<td>In-Sensor and In-Memory Computing for Constrained Hardware for TinyML IoT Applications</td>
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<td>Kea-Tiong Tang, National Tsing Hua University, Hsinchu, Taiwan</td>
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<td>3:05 PM</td>
<td>Break</td>
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<tr>
<td>3:20 PM</td>
<td>Nonvolatile Logic and Smart Nonvolatile Processors with CMOS/MTJ Hybrid Technology for IoT and AI (AIoT) Edge System</td>
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<td>Tetsuo Endoh, Tohoku University, Sendai, Japan</td>
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<td>4:10 PM</td>
<td>How TensorFlow Enables the TinyML Ecosystem</td>
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<td>Raziel Alvarez, Google, Mountain View, CA</td>
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<td>5:00 PM</td>
<td>Concluding Remarks,</td>
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<tr>
<td></td>
<td>Dennis Sylvester, University of Michigan, Ann Arbor, MI</td>
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</table>
The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of approximately 21 ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Machine Learning & Digital; Biomedical & Analog; Communications & RF.

The Student Research Preview will include an inspirational lecture by Professor Tadahiro Kuroda. The SRP begins at 7:30 pm on Sunday, February 16th. The SRP is open to all ISSCC registrants.

**EE1:  Student Research Preview (SRP)**

**Co-Chair:** Denis Daly  
Omni Design Technologies, Billerica, MA

**Co-Chair:** Jerald Yoo  
National University of Singapore, Singapore

**Secretary:** Tinoosh Mohsenin  
University of Maryland, Baltimore, MD

**Advisor:** Anantha Chandrakasan  
MIT, MA

**Advisor:** Jan Van der Spiegel  
University of Pennsylvania, PA

**Media/Publications:** Laura Fujino  
University of Toronto, Canada

**A/V:** Trudy Stetzler  
Halliburton, Houston, TX

**COMMITTEE MEMBERS**

<table>
<thead>
<tr>
<th>Name</th>
<th>Affiliation</th>
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<tr>
<td>Jason Anderson</td>
<td>University of Toronto, Canada</td>
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<td>Masoud Babaie</td>
<td>Delft University of Technology, The Netherlands</td>
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<td>Andrea Baschirotto</td>
<td>University of Milan-Bicocca, Italy</td>
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<td>Hsin-Shu Chen</td>
<td>National Taiwan University, Taiwan</td>
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<td>Hayun Chung</td>
<td>Korea University, Korea</td>
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<td>Denis Daly</td>
<td>Omni Design Technologies, MA</td>
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<td>Shidhartha Das</td>
<td>Arm, United Kingdom</td>
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<td>Zeynep Deniz</td>
<td>IBM, NY</td>
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<td>Hao Gao</td>
<td>Eindhoven University of Technology, The Netherlands</td>
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<td>Minkyu Je</td>
<td>KAIST, Korea</td>
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<td>Matthias Kuhl</td>
<td>Hamburg University of Technology, Germany</td>
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<td>Seulki Lee</td>
<td>imec-Netherlands, The Netherlands</td>
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<td>Yoonmyung Lee</td>
<td>SungKyunKwan University, Korea</td>
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<td>Qiang Li</td>
<td>University of Electronic Science &amp; Technology, China</td>
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<td>Shih-Chii Liu</td>
<td>University of Zurich/ETH Zurich, Switzerland</td>
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<td>Carolina Mora Lopez</td>
<td>IMEC, Belgium</td>
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<td>Shahriar Mirabbasi</td>
<td>University of British Columbia, Canada</td>
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<td>Tinoosh Mohsenin</td>
<td>University of Maryland, MD</td>
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<td>Cormac O’Connell</td>
<td>TSMC, Kanata, Canada</td>
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<td>Mondira Pant</td>
<td>Intel, MA</td>
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<td>Negar Reiskarimian</td>
<td>MIT, MA</td>
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<td>Jae-sun Seo</td>
<td>Arizona State University, AZ</td>
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<td>Atsushi Shirane</td>
<td>Tokyo Institute of Technology, Japan</td>
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<td>Yildiz Sinangil</td>
<td>Apple, CA</td>
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<td>GuoXing Wang</td>
<td>Shanghai Jiao Tong University, China</td>
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<td>Jeffrey Weldon</td>
<td>University of Hawaii, HI</td>
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<td>Chia-Hsiang Yang</td>
<td>National Taiwan University, Taiwan</td>
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<td>Rabia Tugce Yazicigil</td>
<td>Boston University, MA</td>
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<td>Jerald Yoo</td>
<td>National University of Singapore, Singapore</td>
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<td>Samira Zaliasl</td>
<td>Ferric, NY</td>
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<td>Milin Zhang</td>
<td>Tsinghua University, Beijing, China</td>
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EE2: Rising Stars 2020 Workshop

Chair: Farhana Sheikh, Intel, Hillsboro, OR
Co-Chair: Rabia Yazicigil, Boston University, Boston, MA

Rising Stars 2020 Workshop Committee:
Zeynep Deniz, IBM
Dina R. El-Damak, University of Southern California
Q. Jane Gu, University of California, Davis
Ulkuhan Guler, Worcester Polytechnic Institute
Alicia Klinefelter, NVIDIA
Rikky Muller, University of California, Berkeley
Negar Reiskarimian, MIT
Yildiz Sinangil, Apple
Trudy Stetzler, Halliburton
Alice Wang, Everactive
Kathy Wilcox, AMD

Advisory Board:
Tsu-Jae K. Liu, U. C. Berkeley
Andrea Goldsmith, Stanford University
Anantha Chandrakasan, MIT

The IEEE SSCS Women in Circuits together with ISSCC will be sponsoring the first “Rising Stars 2020” for young professionals and students. The Rising Stars 2020 is an educational workshop for graduate and undergraduate students, and young professionals who have graduated within the last two years who are interested in learning how to excel at academic and industry careers in computer science, computer and electrical engineering. “Rising to the Top in Industry” career panel will touch upon topics such as mentoring, setting career goals, filing patents, management vs. technical tracks, and more. “Navigating the Assistant Professorship” will address applying for a faculty position, tenure review, and managing day-to-day life in academia. The panels are open to the all ISSCC 2020 attendees and the public. In addition to the panels, we will be selecting 20 rising stars in academia and industry to attend a special dinner, keynote from a high-profile already “Risen Star”, and mentoring session.

EVENING EVENT Sunday February 16th, 4:00 PM

EE2: Rising Stars 2020 Workshop

Welcome, Introductions, Posters, Networking, and Photos
Dinner, Keynote, and Mentoring
Navigating the Assistant Professorship (Open to the public)
Rising to the Top in Industry (Open to the Public)

Welcome, Posters, and Networking

Workshop Opening and Introduction
Farhana Sheikh, Intel and Rabia Yazicigil, Boston University

Poster Introductions
Presented by Rising Stars

Networking

Time Rising Stars 2020
4:00 – 5:00 PM Welcome, Introductions, Posters, Networking, and Photos
5:00 – 6:30 PM Dinner, Keynote, and Mentoring
6:30 - 7:30 PM Navigating the Assistant Professorship (Open to the public)
6:30 - 7:30 PM Rising to the Top in Industry (Open to the Public)

4:00PM – 5:00PM
Welcome, Posters, and Networking

4:00PM – 5:10PM
Workshop Opening and Introduction
Farhana Sheikh, Intel and Rabia Yazicigil, Boston University

4:10PM – 4:30PM
Poster Introductions
Presented by Rising Stars

4:30PM – 5:00PM
Networking
Rising Stars 2020 Dinner, Keynote, and Mentoring

5:00PM – 5:30PM
Introductions and Dinner
Farhana Sheikh, Intel and Kathy Wilcox, AMD

5:30PM – 6:00PM
Rising Stars 2020 Workshop Dinner Keynote (closed to selected Rising Stars)
Speaker: Anantha Chandrakasan, MIT

6:00PM – 6:30PM
Rising Stars 2020 Workshop Mentoring Session (closed to selected Rising Stars)

6:30PM – 7:30PM
Navigating the Assistant Professorship - Academia Career Panel (open to the public)

Distinguished Panel Speaker:
“Words of Wisdom”, Azita Emami, California Institute of Technology

The panel will provide perspectives from professors and rising stars in the academic field on the faculty application process, the necessary steps to increase your chances of being hired, and the requirements at the tenure review. The panel will provide participants with practical information and candid advice on seeking and interviewing for faculty jobs, networking, teaching, speaking, mentoring, funding research, setting up labs, getting tenure, and managing day-to-day life in academia.

Panel Moderators: Dina Reda El-Damak, University of Southern California
Q. Jane Gu, University of California, Davis

Panelists:
Vivienne Sze, MIT
Esther Rodriguez Villegas, Imperial College, London, UK
Jerald Yoo, National University of Singapore
Zhengya Zhang, University of Michigan
Milin Zhang, Tsinghua University

6:30PM – 7:30PM
Rising to the Top in Industry - Industry Career Panel (Open to the Public)

Distinguished Panel Speaker
“Words of Wisdom”, Alice Wang, VP, Everactive

The industry career panel will tackle the question of how to become a rising star in the corporate world. Our diverse panelists bring their own experiences and perspectives from small startup organizations to large corporations, including corporate research labs. The panel will touch upon topics such as mentoring, setting career goals, deciding between management and technical tracks, publishing and filing patents, collaborating across diverse teams, and working effectively in a team. The goal is to provide the audience with the know-how to successfully navigate challenges in the corporate world, and rise to the top.

Panel Moderators: Alicia Klinefelter, NVIDIA
Zeynep Deniz, IBM

Panelists:
Wendy Belluomini, IBM
Mike Mulligan, Silicon Labs
Kazuko Nishimura, Panasonic
Walker Turner, NVIDIA
Laura Fick, Mythic AI
Plenary Session — Invited Papers

Chair: Jan van der Spiegel, University of Pennsylvania, Philadelphia, PA
ISSCC Conference Chair

Associate Chair: Un-Ku Moon, Oregon State University, Corvallis, OR
ISSCC International Technical Program Chair

FORMAL OPENING OF THE CONFERENCE 8:30 AM

1.1 The Deep Learning Revolution and Its Implications for Computer Architecture and Chip Design

Jeff Dean, Google, Mountain View, CA

The past decade has seen a remarkable series of advances in machine learning, and in particular deep learning approaches based on artificial neural networks, to improve our abilities to build more accurate systems across a broad range of areas, including computer vision, speech recognition, language translation, and natural language understanding tasks. In this talk, I will highlight some of these advances, and their implications on the kinds of computational devices we need to build, especially in an era where general purpose computers are no longer improving their performance significantly year-over-year. I’ll also discuss some of the ways that machine learning may also be able to help with some aspects of the circuit design process. Finally, I’ll provide a sketch of at least one interesting direction towards much larger-scale multi-task models that are sparsely activated and employ much more dynamic, example- and task-based routing than the machine learning models of today.

1.2 Fertilizing AIoT from Roots to Leaves

Kou-Hung Lawrence Loh, MediaTek, Hsinchu, Taiwan

Artificial intelligence (AI) creates new opportunities for all kinds of “things” to interface with the universe in unprecedented ways. As IC technology advances, AI has evolved from traditional expert systems toward cognitive intelligence, which involves multidimensional perception, self-learning, decision-making, and interaction. Enabling cognitive AI in everything (AIoT) demands comprehensive circuit technologies to enhance the performance, power dissipation, and form factor of edge devices as well as cloud infrastructure, which forms the roots to support a variety of leaf-applications. The root-technologies are far ranging, including AI Processing Unit (APU), multi-processor computing, 5G, high-speed wireline communication between edge and the cloud, emerging storage technology, human-machine interfaces, and advanced SoC packages. These fundamental technologies enable intelligent applications spanning across mobile devices, smart home, automotive platform, and smart city. This talk will discuss the advancement of these root technologies that are driving the current transition from conventional ICs to AIoT. Through the discussion, technical innovations for Edge AI SoC and Cloud-Edge collaboration enabled by emerging wireless and wireline communication standards will be explored. To reach the vision of over 350 billion connected intelligent devices in 2030, the challenges and opportunities for our industry going forward will be summarized.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS 9:55 AM

BREAK 10:20 AM
In a smart society where everything will be connected, an avalanche of data is coming toward us, with numbers going to several hundreds of zettabytes per year by 2025. This data will need to be sent around, stored, computed and analyzed. At the heart of it all will be innovations at the technology and system level. With Moore's law under pressure, a rethinking of what the semiconductor industry calls scaling will be needed.

In this work, we will show the strong push to technology diversification, blending different technologies together to achieve benefits at the system level. This brings the interaction of technology and design to the next level: System-Technology co-optimization (STCO), with 3D technologies taking a central stage. Furthermore, the growing demand for storage will put an increasing pressure on the memory hierarchy where emerging concepts like MRAM, FeFET... have the potential to bring new speed and capacity benefits. Next to that, memories like e.g. RRAM are getting a lot of traction for analog in-memory computing to enable energy efficient machine learning at the IoT edge. Finally, we will also briefly review the status of quantum computing, these days gaining a lot of interest as a path to ultra-powerful computing.

The laptops, cell phones, and internet applications commonplace in our daily lives are all rooted in the idea of zeros and ones – in bits.

This foundational element originated from the combination of mathematics and Claude Shannon's Theory of Information. Coupled with the 50-year legacy of Moore's law, the bit has propelled the digitization of our world.

In recent years, artificial intelligence systems, merging neuron-inspired biology with information, have achieved superhuman accuracy in a range of narrow classification tasks by learning from labelled data. Advancing from narrow AI to broad AI will encompass the unification of learning and reasoning through neuro-symbolic systems, resulting in a form of AI which will perform multiple tasks, operate across multiple domains, and learn from small quantities of multi-modal input data.

Finally, the union of physics and information led to the emergence of Quantum Information Theory and the development of the quantum bit - the qubit - forming the basis of quantum computers. We have built the first programmable quantum computers, and although the technology is still in its early days, these systems offer the potential to solve problems which even the most powerful classical computers cannot.

The future of computing will look fundamentally different that it has in the past. It will not be based on more and cheaper bits alone, but rather, it will be built upon bits + neurons + qubits. This future will enable the next generation of intelligent mission critical systems and accelerate the rate of science-driven discovery.
1.30 PM

2.1 Zen 2: The AMD 7nm Energy-Efficient High-Performance x86-64 Microprocessor Core
T. Singh1, S. Rangarajan1, D. John1, R. Schreiber1, S. Oliver1, R. Seahra1, A. Schaefer1
AMD, Austin, TX; 2AMD, Markham, ON, Canada

2.2 AMD Chiplet Architecture for High-Performance Server and Desktop Products
S. Naftziger1, K. Lepak2, M. Paraschou1, M. Subramony2
AMD, Fort Collins, CO; 2AMD, Austin, TX

2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm2 Inter-Chiplet Interconnects and 156mW/mm2 @ 82%-Peak-Efficiency DC-DC Converters
P. Vivet1, E. Guthmuller1, Y. Thonnart1, G. Pillionet1, M. Moritz1, I. Miro-Paradis2, C. Fuguet1, J. Durup1, C. Bernard1, D. Varreau1, J. Pontes1, S. Thune1, D. Coriat1, M. Harrand1, D. Dutillot1, D. Lattard1, L. Arnaud1, J. Charbonnier1, P. Coudrain1, A. Garnier1, F. Berger1, A. Gueugnot1, A. Greiner1, Q. Meunier2, A. Farcy2, A. Arriordaz3, S. Cheramy2, E. Clermidy1
CEA-LETI-MINATEC, Grenoble, France; 2Sorbonne University, Paris, France; 3STMicroelectronics, Crolles, France; 4Mentor, St. Ismier, France

3:00 PM Break

3:15 PM

2.4 A 7nm High-Performance and Energy-Efficient Mobile Application Processor with Tri-Cluster CPUs and a Sparsity-Aware NPU
Samsung Electronics, Hwaseong, Korea

3:45 PM

2.5 A 7nm FinFET 2.5GHz/2.0GHz Dual-Gear Octa-Core CPU Subsystem with Power/Performance Enhancements for a Fully Integrated 5G Smartphone SoC
H. Mair1, E. Wang2, A. Naya1, R. Lagerquist1, L. Chou2, G. Gammie2, H. Chen2, L-K. Yong2, M. Rahman2, J. Wiedemeier1, R. Madhavaram2, A. Chiu2, B. Li2, V. Lin2, R. Huang2, M. Yang2, A. Thippana2, O. Su2, S. Huang2, MediaTek, Austin, TX; 2MediaTek, Hsinchu, Taiwan

4:15 PM

2.6 A 16nm 3.5B Transistor >14TOPS 2-to-10W Multicore SoC Platform for Automotive and Embedded Applications with Integrated Safety MCU, 512b Vector VLIW DSP, Embedded Vision and Imaging Acceleration
R. Venkatasubramanian2, D. Steiss1, G. Shurtz2, T. Anderson2, K. Chirca2, R. Santhanagopalan2, N. Nandani1, A. Reghunath1, H. Sanghvi1, D. Wu1, A. Chachak1, B. Karguth1, D. Beaudoin2, C. Fuoco1, L. Nardini1, C. Hu1, V. Visalili2, A. Muntra1, D. Varadarajan1, F. Cano2, S. Stelmach1, M. Modly1, A. Redfern1, H. Bilhan1, M. Sarraj1, A. Siddiki1, A. Leli1, E. Falik1, A. Hill1, A. Armstrong1, T. Beck1, V. Kanumuri1, S. Mullinnix1, D. Moore1, J. Jones1, M. Koul1, S. Agarwala1
Texas Instruments, Dallas, TX; 2Texas Instruments, Houston, TX; 3Texas Instruments, Bangalore, India

4:45 PM

2.7 IBM z15: A 12-Core 5.2GHz Microprocessor
C. Berry1, B. Bell2, A. Jakowski1, J. Surprise1, J. Isaksen2, O. Geva3, B. Deskin3, M. Cichanowski3, D. Hamid1, C. Cavitt1, G. Federman1, A. Saporito1, A. Mishra2, A. Buyuktosunoglu2, T. Weber2, P. Lobo2, P. Parashuraman2, R. Bertrand2, D. Chidambaram2, D. Wolpert2, B. Bruen2
IBM Systems and Technology, Poughkeepsie, NY; 2IBM Systems and Technology, Rochester, NY; 3IBM Systems and Technology, Austin, TX; 4IBM Systems and Technology, Endicott, NY; 5IBM Systems and Technology, Bangalore, India; 6IBM Systems and Technology, London, UK; 7T.J. Watson Research Center, Yorktown Heights, NY; 8IBM Systems and Technology, Boeblingen, Germany; 9IBM Systems and Technology, Yorktown Heights, NY; 10IBM Systems and Technology, Hopewell Junction, NY

5:15 PM Conclusion
Analog Techniques I

Session Chair: Youngcheol Chae, Yonsei University, Seoul, Korea
Session Co-Chair: Michael Perrott, Texas Instruments, Manchester, NH

1:30 PM

3.1 An Integrated BAW Oscillator with \( <30 \text{ppm} \) Frequency Stability Over Temperature, Package Stress, and Aging Suitable for High-Volume Production

D. Griffith\(^1\), E. T-T. Yen\(^2\), K. Tsai\(^1\), H. U. R. Mohammed\(^1\), B. Haroun\(^1\), A. Kiae\(^2\), A. Baha\(^2\)
\(^1\)Texas Instruments, Dallas, TX; \(^2\)Texas Instruments, Santa Clara, CA

2:00 PM

3.2 A 0.0088mm\(^2\) Resistor-Based Temperature Sensor Achieving 92IJ-K\(^2\) FoM in 65nm CMOS

A. Khashaba, J. Zhu, A. Elmallah, M. Ahmed, P. Hanumolu
University of Illinois, Urbana, IL

2:30 PM

3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection

L. Xu\(^1\), T. Jang\(^2\), J. Lim\(^1\), K. Choo\(^1\), D. Blaauw\(^1\), D. Sylvester\(^1\)
\(^1\)University of Michigan, Ann Arbor, MI; \(^2\)ETH Zürich, Zürich, Switzerland

3:15 PM

3.4 A 16MHz CMOS RC Frequency Reference with \( \pm400 \text{ppm} \) Inaccuracy from -45°C to 85°C after Digital Linear Temperature Compensation

Ç. Gürleyük, S. Pan, K.A.A. Makinwa
Delft University of Technology, Delft, The Netherlands

3:45 PM

3.5 A 34μW 32MHz RC Oscillator with \( \pm530 \text{ppm} \) Inaccuracy from -40°C to 85°C and 80ppm/V Supply Sensitivity Enabled by Pulse-Density Modulated Resistors

University of Illinois, Urbana, IL

4:15 PM

3.6 A CMOS Resistor-Based Temperature Sensor with a 10IJ-K\(^2\) Resolution FoM and 0.4°C (3\(\sigma\)) Inaccuracy From -55°C to 125°C After a 1-point Trim

S. Pan, K.A.A. Makinwa, Delft University of Technology, Delft, The Netherlands

4:45 PM

3.7 A 620µW BJT-Based Temperature-to-Digital Converter with 0.65mK Resolution and FoM of 190fJ·K\(^2\)

S. Heidary Shalmany\(^1\), K. Souri\(^1\), U. Sonmez\(^2\), K. Souri\(^2\), M. D’Urbino\(^1\), S. Hussaini\(^3\), D. Tauro\(^2\), S. Tabatabaei\(^2\)
\(^1\)SiTime, Delft, The Netherlands; \(^2\)SiTime, Santa Clara, CA

5:00 PM

3.8 A 23.6ppm/°C Monolithically Integrated GaN Reference Voltage Design with Temperature Range from -50°C to 200°C and Supply Voltage Range from 3.9 to 24V

C.-H. Liao\(^1\), S.-H. Yang\(^1\), M.-Y. Liao\(^1\), K.-C. Chung\(^1\), N. Kumari\(^1\), K.-H. Chen\(^1\), Y.-H. Lin\(^2\), S.-R. Lin\(^2\), T.-Y. Tsa\(^2\), Y.-Z. Juang\(^4\)
\(^1\)National Chiao Tung University, Hsinchu, Taiwan
\(^2\)Realtek Semiconductor, Hsinchu, Taiwan
\(^3\)Realtek Semiconductor, Hsinchu City, Taiwan
\(^4\)Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan

Conclusion 5:15 PM
4.1 A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications

4.2 An E-Band High-Linearity Antenna-LNA Front-End with 4.8dB NF and 2.2dBm IIP3 Exploiting Multi-Feed On-Antenna Noise-Canceling and $G_m$-Boosting
S. Li1, T. Chi2, D. Jung1, T-Y. Huang1, M-Y. Huang1, H. Wang1
1Georgia Institute of Technology, Atlanta, GA; 2Rice University, Houston, TX

4.3 A 28GHz 4-Element MIMO Beam-Space Array in 65nm CMOS with Simultaneous Spatial Filtering and Single-Wire Frequency-Domain Multiplexing
R. Garg1, G. Sharma*1, A. Binaie*2, S. Jain*1, S. Ahasan*2, A. Dascuurcu*2, H. Krishnaswamy*2, A. Natarajan*1
*Equally-Credited Authors (ECAs), 1Oregon State University, Corvallis, OR; 2Columbia University, New York, NY

4.4 A 28/37GHz Scalable, Reconfigurable Multi-Layer Hybrid/Digital MIMO Transceiver for TDD/FDD and Full-Duplex Communication
S. Mondal, L. R. Carley, J. Paramesh, Carnegie Mellon University, Pittsburgh, PA

Break 3:00 PM

4.5 A 64Gb/s 1.4pJ/b/element 60GHz 2×2-Element Phased-Array Receiver with 8b/symbol Polarization MIMO and Spatial Interference Tolerance
A. Chakrabarti, C. Thakkar, S. Yamada, D. Choudhury, J. Jaussi, B. Casper, Intel, Hillsboro, OR

3:45 PM

4.6 Space-Time Modulated 71-to-76GHz mm-Wave Transmitter Array for Physically Secure Directional Wireless Links
X. Lu*1, S. Venkatesh*1, B. Tang*2, K. Sengupta*1, *Equally-Credited Authors (ECAs), 1Princeton University, Princeton, NJ; 2Xi’an Jiaotong University, Xi’an, China

4:15 PM

4.7 A Single-Antenna W-Band FMCW Radar Front-End Utilizing Adaptive Leakage Cancellation
M. Kalantari1,2, H. Shirinabadi1, A. Fotowat-Ahmadi1, C. P. Yue1
1Hong Kong University of Science and Technology, Hong Kong, China; 2Sharif University of Technology, Tehran, Iran; 3University of California, Berkeley, CA

4:45 PM

4.8 A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth
X. Yi1, C. Wang1, M. Lu1, J. Wang1, J. Grafali1,2, R. Han1
1Massachusetts Institute of Technology, Cambridge, MA; 2Universidad Politécnica de Madrid, Madrid, Spain

Conclusion 5:15 PM
Imagers and ToF Sensors

Session Chair: Seong-Jin Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea
Session Co-Chair: Hayato Wakabayashi, Sony Semiconductor Solutions, Atsugi, Japan

5.1  A 240×192Pixel 10fps 70lux 225m-Range Automotive LiDAR SoC Using a 40ch 0.0036mm² Voltage/Time Dual-Data-Converter-Based AFE
S. Kondo¹, H. Kubota¹, H. Katagiri¹, Y. Ota¹, M. Hiroto¹, T. T. Ta¹, H. Okuni¹, S. Ohtsuka², Y. Ojima³, T. Sugimoto¹, H. Ishii⁴, K. Yoshioka⁴, K. Kimura⁴, A. Sai⁵, N. Matsumoto⁵, Toshiba, Kawasaki, Japan
¹Toshiba Electronic Devices & Storage, Kawasaki, Japan; ²Toshiba, Yokohama, Japan

5.2  A 1200×900 6μm 450fps Geiger-Mode Vertical Avalanche Photodiodes CMOS Image Sensor for a 250m Time-of-Flight Ranging System Using Direct-Indirect-Mixed Frame Synthesis with Configurable-Depth-Resolution Down to 10cm

5.3  An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform

5.4  A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120klux
D. Kim¹, S. Lee², D. Park², C. Piao³, J. Park³, Y. Ahn³, K. Cho¹, J. Sim³, S. M. Song³, S-J. Kim², J-H. Chun¹, J. Choi³, *Sungkyunkwan University, Suwon, Korea
¹Ulsan National Institute of Science and Technology, Ulsan, Korea; ²Zeetam, Hanam, Korea

5.5  A 2.1e⁻ Temporal Noise and -105dB Parasitic Light Sensitivity Backside-Illuminated 2.3 μm-Pixel Voltage-Domain Global Shutter CMOS Image Sensor Using High-Capacity DRAM Capacitor Technology

5.6  A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7µm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology

5.7  A 132dB Single-Exposure-Dynamic-Range CMOS Image Sensor with High Temperature Tolerance
Y. Sakano¹, T. Toyoshima¹, R. Nakamura¹, T. Asatsuma¹, Y. Hattori¹, T. Yamanaka², R. Yoshikawa², N. Kawazu¹, T. Matsoura¹, T. Iinuma¹, T. Toyofuku¹, A. Kato¹, Y. Oike¹
¹Sony Semiconductor Manufacturing, Kikuyo, Japan
²Sony Semiconductor Solutions, Atsugi, Japan

5.8  A 0.50e rms Noise 1.45μm-Pitch CMOS Image Sensor with Reference-Shared In-Pixel Differential Amplifier at 8.3Mpixel 35fps
Sony Semiconductor Solutions, Atsugi, Japan

5.9  A 0.8V Multimode Vision Sensor for Motion and Salience Detection with Ping-Pong PWM Pixel
T-H. Hsu¹, Y-K. Chen¹, J-S. Wu, W-C. Ting, C-T. Wang, C-F. Yeh, S-H. Sie, Y-R. Chen, R-S. Liu, C-C. Lo, K-T. Tang, M-F. Chang, C-C. Hsieh¹, *Equally-Credited Authors (ECAs)
National Tsing Hua University, Hsinchu, Taiwan
¹Sony Semiconductor Manufacturing, Kikuyo, Japan

5.10  A 1280×720 Back-Illuminated Stacked Temporal Contrast Event-Based Vision Sensor with 4.86μm Pixels, 1.06GEPs Readout, Programmable Event-Rate Controller and Compressive Data-Formatting Pipeline
T. Finatet¹, A. Niiwa², D. Matolín³, K. Tsuchimoto³, A. Mascheroni³, E. Reynaud³, P. Mostafalu³, F. Brady³, L. Chotard³, F. LeGoff³, H. Takahashi³, H. Wakabayashi³, Y. Oike³, C. Posch³
¹PROPHESEE, Paris, France; ²Sony Semiconductor Solutions, Atsugi, Japan
³Sony Electronics, Rochester, NY

Conclusion 5:15 PM
6.1 A 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET

J. Im1, K. Zhong1, A. Chou1, L. Zhou1, J. W. Kim1, S. Chen1, Y. Wang2, H-W. Hung2, K. Tan2, W. Lin4, A. Roldan1, D. Carey3, R. Casey3, A. Bekele1, Y. Cao1, D. Mahashin1, H. Ahn1, H. Zhang4, Y. Frans1, K. Chang5

1Xilinx, San Jose, CA; 2Xilinx, Singapore; 3Xilinx, Cork, Ireland

2:00 PM

6.2 A 460mW 112Gb/s DSP-Based Transceiver with 38dB Loss Compensation for Next-Generation Data Centers in 7nm FinFET Technology

T. Ali*1, E. Chen*1, H. Park*1, R. Yousry*1, Y-M. Ying1, M. Abdullatif1, M. Gandara1, C-C. Liu2, P-S. Weng2, H-S. Chen1, M. Elbadry1, Q. Nehal1, K-H. Tsai2, K. Tan2, Y-C. Huang2, C-H. Tsai2, Y. Chang2, Y-H. Tung2

*Equally-Credited Authors (ECAs), 1MediaTek, Irvine, CA; 2MediaTek, Hsinchu, Taiwan

2:30 PM

6.3 A 10-to-112Gb/s DSP-DAC-Based Transmitter with 1.2Vpp Output Swing in 7nm FinFET

E. Groen1, C. Boecker1, M. Hossain2, R. Vu1, S. Vamvakos1, H. Lin1, S. Li1, M. van Ierssel3, P. Choudhary1, N. Wang1, M. Shibata2, M. H. Taghavi2, N. Nguyen1,4, S. Desai1

1Rambus, Sunnyvale, CA; 2University of Alberta, Edmonton, Canada; 3Rambus, Toronto, Canada; 4San Jose State University, San Jose

Break 3:00 PM

3:15 PM

6.4 A 56Gb/s 7.7mW/Gb/s PAM-4 Wireline Transceiver in 10nm FinFET Using MM-CDR-Based ADC Timing Skew Control and Low-Power DSP with Approximate Multiplier


3:45 PM

6.5 A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS

K. Park, M. Shim, H-G. Ko, D-K. Jeong, Seoul National University, Seoul, Korea

4:15 PM

6.6 Reference-Noise Compensation Scheme for Single-Ended Package-to-Package Links


1NVIDIA, Santa Clara, CA; 2NVIDIA, Durham, NC

4:45 PM

6.7 An 8Gb/s/μm FFE-Combined Crosstalk-Cancellation Scheme for HBM on Silicon Interposer with 3D-Staggered Channels

H-G. Ko, S. Shin, J. Oh, K. Park, D-K. Jeong, Seoul National University, Seoul, Korea

5:00 PM

6.8 A 100Gb/s NRZ Transmitter with 8-Tap FFE Using a 7b DAC in 40nm CMOS

P-J. Peng1, S-T. Lai2, W-H. Wang1, C-W. Lin1, W-C. Huang1, T. Shih2

1Yuan Ze University, Taoyuan, Taiwan; 2Teletrx, Taipei, Taiwan

Conclusion 5:15 PM
This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2020, as noted by the symbol DS1.

2.1 Zen 2: The AMD 7nm Energy-Efficient High-Performance x86-64 Microprocessor Core

3.1 An Integrated BAW Oscillator with ≤30ppm Frequency Stability Over Temperature, Package Stress, and Aging Suitable for High-Volume Production

3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection

4.7 A Single-Antenna W-Band FMCW Radar Front-End Utilizing Adaptive Leakage Cancellation

4.8 A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth

5.1 A 240×192Pixel 10fps 70kLux 225m-Range Automotive LiDAR SoC Using a 40ch 0.0036mm² Voltage/Time Dual-Data-Converter-Based AFE

5.2 A 1200×900 6µm 450fps Geiger-Mode Vertical Avalanche Photodiodes CMOS Image Sensor for a 250m Time-of-Flight Ranging System Using Direct-Indirect-Mixed Frame Synthesis with Configurable-Depth-Resolution Down to 10cm

5.3 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform

5.4 A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120kLux

5.10 A 1280×720 Back-Illuminated Stacked Temporal Contrast Event-Based Vision Sensor with 4.86µm Pixels, 1.066GEPS Readout, Programmable Event-Rate Controller and Compressive Data-Formatting Pipeline

6.1 An 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET

6.2 A 460mW 112Gb/s DSP-Based Transceiver with 38dB Loss Compensation for Next-Generation Data Centers in 7nm FinFET Technology

6.3 A 10-to-112Gb/s DSP-DAC-Based Transmitter with 1.2Vpp Output Swing in 7nm FinFET

28.3 A 5.2Mpixel 88.4dB-DR 12in CMOS X-Ray Detector with 16b Column-Parallel Continuous-Time ΔΣ ADCs

28.4 A CMOS Multimodality In-Pixel Electrochemical and Impedance Cellular Sensing Array for Massively Parallelized Synthetic Exoelectrogen Characterization

29.1 Non-Magnetic 0.18μm SOI Circulator with Multi-Watt Power Handling Based on Switched-Capacitor Clock Boosting

29.4 A CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers

30.6 A Low-Power BLE Transceiver with Support for Phase-Based Ranging, Featuring 5µs PLL Locking Time and 5.3Ms Ranging Time, Enabled by Staircase-Chirp PLL with Sticky-Lock Channel-Switching

34.1 A 64×64 Implantable Real-Time Single-Charged-Particle Radiation Detector for Cancer Therapy

34.2 1225-Channel Localized Temperature-Regulated Neuromorphic Retinal-Prosthesis SoC with 56.3nW/Channel Image Processor

34.6 EEG Dust: A BCC-Based Wireless Concurrent Recording/Transmitting Concentric Electrode
ISSCC will hold a plenary Industry Showcase event on the evening of Monday, February 17th, which will highlight how advances in silicon circuits, SoCs and systems are fueling the most innovative industrial applications and products of the future. Following the recognized role of ISSCC as the foremost global forum for advances in solid-state circuits and systems-on-chip (SoCs), the goal of this event will be to highlight the role of silicon in the creation of novel products. It will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation. The featured presentations were chosen through a nomination and voting process by members of the Industry Showcase Committee and represent an exciting introduction to the next generation of applications and products enabled by the sustained evolution of solid-state integrated circuits.

**Amongst those participating will be:**

- **Intel** (Lakefield: Hybrid Computing with 3D silicon integration)
- **Wiliot** (Low-Cost Bluetooth Based Sensor Tags for IoT)
- **IBM** (IBM Z15 – A 12 Core 5.2GHz Microprocessor)
- **Butterly Network** (Handheld Whole-Body Imager with Ultrasound-on-Chip)
- **Weebit Nano** (Spiking Neural Network using ReRAM)
- **Samsung Semiconductor** (Motion-resilient VGA Time-of-Flight Image Sensor)
- **Samsung Electronics** (A 1/1.33-inch 108MP CMOS Image Sensor with 0.8µm Unit Pixels)
- **Samsung Electronics** (A Blocker-Tolerant Direct Sampling Receiver for Wireless Multi-Channel Communication)
- **Ferric** (Fully Programmable Power Converter Chiplet using Ferric Integrated Inductors)
- **Texas Instruments** (Camera Based Perception and 3D Surround View for Autonomous Valet Parking on a 16nm Automotive SoC)
- **Advanced Micro Devices** (AMD Radeon RX5700 Graphics Power and Performance Demonstration)
- **Western Digital Research** (A Vehicle Security Surveillance Based on Artificial Intelligence of Things (AlOT))
- **MediaTek** (A Dual Core Deep Learning Accelerator for Versatile AI Applications in a 7nm 5G Smartphone SoC)
- **Alibaba** (Hanguang 800, a High Throughput AI Inference Chip)
High-Performance Machine Learning
Session Chair: Geoffrey Burr, IBM Research Almaden, San Jose, CA
Session Co-Chair: Yan Li, Western Digital, Milpitas, CA

8:30 AM

7.1 A 3.4-to-13.3TOPS/W 3.6TOPS Dual-Core Deep-Learning Accelerator for Versatile AI Applications in 7nm 5G Smartphone SoC
MediaTek, Hsinchu, Taiwan

9:00 AM

7.2 A 12nm Programmable Convolution-Efficient Neural-Processing-Unit Chip Achieving 825TOPS
1Alibaba, Sunnyvale, CA
2Alibaba, Seattle, WA
3Alibaba, Shanghai, China
4Alibaba, Hangzhou, China

9:15 AM

7.3 STATICA: A 512-Spin 0.25M-Weight Full-Digital Annealing Processor with a Near-Memory All-Spin-Updates-at-Once Architecture for Combinatorial Optimization with Complete Spin-Spin Interactions
K. Yamamoto1,2, K. Ando1, N. Mertig3, T. Takemoto2, M. Yamaoka3, H. Teramoto2, A. Sakai1, S. Takamaeda-Yamazaki4, M. Motomura1
1Tokyo Institute of Technology, Yokohama, Japan
2Hokkaido University, Sapporo, Japan
3Hitachi, Sapporo, Japan
4University of Tokyo, Tokyo, Japan

9:30 AM

7.4 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparsity Exploitation
S. Kang, D. Han, J. Lee, D. Im, S. Kim, S. Kim, H-J. Yoo
KAIST, Daejeon, Korea

Break 10:00 AM
10:15 AM

8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm², 1mm Package-on-Package
W. Gomes¹, S. Khushu², D. B. Ingerly¹, P. N. Stover³, N. I. Chowdhury⁴, F. O’Mahony⁵, A. Balankutty⁶, N. Dolev⁷, M. G. Dixon⁸, L. Jiang⁹, S. Prekke¹⁰, B. Patra¹¹, P. V. Rott¹², R. Kumar¹³
¹Intel, Hillsboro, OR
²Intel, Santa Clara, CA
³Intel, Chandler, AZ
⁴Intel, Bangalore, India

10:45 AM

8.2 A Versatile 7nm Adaptive Compute Acceleration Platform Processor
P. K. Raha, T. Knopp, S. Ahmad, A. Ansari, F-H. Ho, T. To, V. Nalluri, M. Sarmah, R. Patwari
Xilinx, San Jose, CA

11:15 AM

8.3 A 3GHz ARM Neoverse N1 CPU in 7nm FinFET for Infrastructure Applications
R. Christy¹, S. Riches², S. Kottekkat³, P. Gopinath⁴, K. Sawant³, A. Kona⁵, R. Harrison⁶
¹ARM, Austin, TX
²ARM, Cambridge, United Kingdom
³ARM, Sheffield, United Kingdom
⁴ARM, Bangalore, India

11:45 AM

8.4 Radeon RX 5700 Series: The AMD 7nm Energy-Efficient High-Performance GPUs
S. Dasgupta¹, T. Singh², A. Jain², S. Naffziger³, D. John³, C. Bisht¹, P. Jayaraman¹
¹AMD, Santa Clara, CA
²AMD, Austin, TX
³AMD, Fort Collins, CO
⁴AMD, Orlando, FL

Conclusion 12:15 PM
9.1 A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s
*Equally-Credited Authors (ECAs)
MediaTek, Hsinchu, Taiwan

9.2 A 134μW 24kHz-BW 103.5dB-DR CT ΔΣ Modulator with Chopped Negative-R and Tri-Level FIR DAC
M. Jang, C. Lee, Y. Chae, Yonsei University, Seoul, Korea

9.3 A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-Order Mismatch Error Shaping
J. Liu¹, X. Wang¹, Z. Gao¹, M. Zhan¹, X. Tang², N. Sun²
¹Tsinghua University, Beijing, China; ²University of Texas, Austin, TX

9.4 A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth
L. Jie, B. Zheng, H-W. Chen, R. Wang, M. P. Flynn
University of Michigan, Ann Arbor, MI

9.5 A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier
X. Tang¹, X. Yang¹, W. Zhao¹, C-K. Hsu¹, J. Liu², L. Shen¹, A. Mukherjee¹, W. Shi¹, D. Z. Pan¹, N. Sun¹
¹University of Texas, Austin, TX; ²Tsinghua University, Beijing, China

9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration
Y. Song¹, Y. Zhu¹, C. H. Chan¹, R. P. Martins¹,²
¹University of Macau, Macau, China; ²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

9.7 Background Multi-Rate LMS Calibration Circuit for 15MHz-BW 74dB-DR CT 2-2 MASH ΔΣ ADC in 28nm CMOS
M. Fukazawa¹, T. Oshima², M. Fujiwara¹, K. Tateyama¹, A. Raed¹, M. Ito¹, T. Matsumoto¹, T. Matsui³
¹Renesas Electronics, Tokyo, Japan; ²Hitachi, Tokyo, Japan

9.8 A Low-Cost 4-Channel Reconfigurable Audio Interface for Car Entertainment Systems
R. van Veldhoven, M. Lammers, L. van der dussen, K. Mabtoul
NXP Semiconductors, Eindhoven, The Netherlands

Conclusion 12:15 PM
High-Performance Transceivers

**Session Chair:** Renaldi Winoto, Mojo Vision, Saratoga, CA
**Session Co-Chair:** Xin He, NXP Semiconductors, Eindhoven, The Netherlands

**8:30 AM**

**10.1** A 1.4-to-2.7GHz FDD SAW-Less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise

G. Qi¹, H. Shao¹, P-I. Mak¹, J. Yin¹, R. P. Martins¹,²
¹University of Macau, Macau, China; ²University of Lisboa, Lisbon, Portugal

**10.2** A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation

S. Su, M. S-W. Chen, University of Southern California, Los Angeles, CA

**8:45 AM**

**10.3** A 12nm CMOS RF Transceiver Supporting 4G/5G UL MIMO

M-D. Tsai¹, S-Y. Yang¹, C-Y. Yu¹, P-Y. Chen¹, T-H. Wu¹, M. Hassan², C-T. Chen¹, C-W. Wang¹, Y-C. Huang¹, L-H. Hung¹, W-H. Chiu¹, A. Lin¹, B-Y. Lin¹, A. Werquin², C-C. Lin¹, Y-H. Chen¹, J-C. Tsai¹, Y-Y. Fu¹, B. Tenbroek², C-S. Chiu¹, Y-B. Lee¹, G-K. Dehng¹, ¹MediaTek, Hsinchu, Taiwan; ²MediaTek, Kent, United Kingdom

**9:00 AM**

**10.4** A 4×4 Dual-Band Dual-Concurrent WiFi 802.11ax Transceiver with Integrated LNA, PA and T/R Switch Achieving +20dBm 1024-QAM MCS11 Pout and -43dB EVM Floor in 55nm CMOS

E. Lu¹, W-K. Li², Z. Deng¹, E. Rostami¹, P-A. Wu², K-M. Chang², Y-C. Huang², C-M. La², Y-C. Chen¹, T-H. Peng², T-C. Tsai², H-H. Liu², C-C. Chiu², B. Huang¹, Y-C. Wang², J-H. C. Zhan², O. Shanaa¹
¹MediaTek, San Jose, CA; ²MediaTek, Hsinchu, Taiwan

**9:15 AM**

**10.5** A Fully Integrated 27dBm Dual-Band All-Digital Polar Transmitter Supporting 160MHz for WiFi 6 Applications

A. Ben-Bassat¹, S. Gross², A. Nazimov³, A. Ravi², B. Khamaisi³, E. Banin², E. Borokhovich⁴, N. Kimiagarov⁴, P. Sklar², R. Banin¹, S. Zur³, S. Reinhold³, S. Bruker², T. Maimon¹, U. Parker², O. Degani³
¹Intel, Haifa, Israel; ²Intel, Petach Tikva, Israel; ³Intel, Hillsboro, OR
⁴Intel, Munich, Germany

**9:30 AM**

**10.6** A 4G/5G Cellular Transmitter in 12nm FinFET with Harmonic Rejection

M-D. Tsai¹, C-W. Tseng¹, K-J. Tsai¹, S. Andrab², P-C. Huang¹, F. Beffa³, Y. Chen³, B. Tenbroek¹, ¹MediaTek, Hsinchu, Taiwan; ²MediaTek, Cambridge, United Kingdom
³MediaTek, Kent, United Kingdom

**9:45 AM**

**10.7** A 0.26mm² DPD-Less Quadrature Digital Transmitter With <-40dB EVM Over >30dB Pout Range in 65nm CMOS

S-W. Yoo¹, S-C. Hung¹, J. S. Walling², D. J. Allstot³, S-M. Yoo¹
¹Michigan State University, East Lansing, MI; ²University of Utah, Salt Lake City, UT
³Oregon State University, Corvallis, OR

**10:00 AM**

**10.8** A 4-Element 500MHz-Modulated-BW 40mW 6b 1GS/s Analog-Time-to-Digital-Converter-Enabled Spatial Signal Processor in 65nm CMOS

E. Ghaderi, C. Puglisi, S. Bansal, S. Gupta, Washington State University, Pullman, WA

**9:00 AM**

**10.2** A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation

S. Su, M. S-W. Chen, University of Southern California, Los Angeles, CA

**9:30 AM**

**10.3** A 12nm CMOS RF Transceiver Supporting 4G/5G UL MIMO

M-D. Tsai¹, S-Y. Yang¹, C-Y. Yu¹, P-Y. Chen¹, T-H. Wu¹, M. Hassan², C-T. Chen¹, C-W. Wang¹, Y-C. Huang¹, L-H. Hung¹, W-H. Chiu¹, A. Lin¹, B-Y. Lin¹, A. Werquin², C-C. Lin¹, Y-H. Chen¹, J-C. Tsai¹, Y-Y. Fu¹, B. Tenbroek², C-S. Chiu¹, Y-B. Lee¹, G-K. Dehng¹, ¹MediaTek, Hsinchu, Taiwan; ²MediaTek, Kent, United Kingdom

**9:45 AM**

**10.4** A 4×4 Dual-Band Dual-Concurrent WiFi 802.11ax Transceiver with Integrated LNA, PA and T/R Switch Achieving +20dBm 1024-QAM MCS11 Pout and -43dB EVM Floor in 55nm CMOS

E. Lu¹, W-K. Li², Z. Deng¹, E. Rostami¹, P-A. Wu², K-M. Chang², Y-C. Huang², C-M. La², Y-C. Chen¹, T-H. Peng², T-C. Tsai², H-H. Liu², C-C. Chiu², B. Huang¹, Y-C. Wang², J-H. C. Zhan², O. Shanaa¹
¹MediaTek, San Jose, CA; ²MediaTek, Hsinchu, Taiwan

**10:00 AM**

**10.5** A Fully Integrated 27dBm Dual-Band All-Digital Polar Transmitter Supporting 160MHz for WiFi 6 Applications

A. Ben-Bassat¹, S. Gross², A. Nazimov³, A. Ravi², B. Khamaisi³, E. Banin², E. Borokhovich⁴, N. Kimiagarov⁴, P. Sklar², R. Banin¹, S. Zur³, S. Reinhold³, S. Bruker², T. Maimon¹, U. Parker², O. Degani³
¹Intel, Haifa, Israel; ²Intel, Petach Tikva, Israel; ³Intel, Hillsboro, OR
⁴Intel, Munich, Germany

**10:15 AM**

**10.6** A 4G/5G Cellular Transmitter in 12nm FinFET with Harmonic Rejection

M-D. Tsai¹, C-W. Tseng¹, K-J. Tsai¹, S. Andrab², P-C. Huang¹, F. Beffa³, Y. Chen³, B. Tenbroek¹, ¹MediaTek, Hsinchu, Taiwan; ²MediaTek, Cambridge, United Kingdom
³MediaTek, Kent, United Kingdom

**10:30 AM**

**10.7** A 0.26mm² DPD-Less Quadrature Digital Transmitter With <-40dB EVM Over >30dB Pout Range in 65nm CMOS

S-W. Yoo¹, S-C. Hung¹, J. S. Walling², D. J. Allstot³, S-M. Yoo¹
¹Michigan State University, East Lansing, MI; ²University of Utah, Salt Lake City, UT
³Oregon State University, Corvallis, OR

**10:45 AM**

**10.8** A 4-Element 500MHz-Modulated-BW 40mW 6b 1GS/s Analog-Time-to-Digital-Converter-Enabled Spatial Signal Processor in 65nm CMOS

E. Ghaderi, C. Puglisi, S. Bansal, S. Gupta, Washington State University, Pullman, WA

**Conclusion 12:15 PM**
DC-DC Converters
Session Chair: Yan Lu, University of Macau, Taipa, Macau
Session Co-Chair: Makoto Takamiya, University of Tokyo, Tokyo, Japan

8:30 AM
11.1 A Direct 12V/24V-to-1V 3W 91.2%-Efficiency Tri-State DSD Power Converter with Online V_CF Rebalancing and In-Situ Precharge Rate Regulation
K. Wei¹, Y. Ramadass², D. B. Ma³
¹University of Texas at Dallas, Richardson, TX
²Texas Instruments, Santa Clara, CA

9:00 AM
11.2 A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator
P. H. McLaughlin, Z. Xia, J. T. Stauth, Dartmouth College, Hanover, NH

9:30 AM
11.3 A One-Step 325V to 3.3-to-10V 0.5W Resonant DC-DC Converter with Fully Integrated Power Stage and 80.7% Efficiency
C. Rindfleisch, B. Wicht, Leibniz University Hannover, Hannover, Germany

Break 10:00 AM

10:15 AM
11.4 A 48-to-80V Input 2MHz Adaptive ZVT-Assisted GaN-Based Bus Converter Achieving 14% Light-Load Efficiency Improvement
Q. Cheng, L. Cong, H. Lee, University of Texas at Dallas, Richardson, TX

10:45 AM
11.5 A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5
M. Huang¹,², Y. Lu¹, R. P. Martins¹,³
¹University of Macau, Macau, China
²South China University of Technology, Guangzhou, China
³University of Lisboa, Lisbon, Portugal

11:15 AM
11.6 A 1.46mm² Simultaneous Energy-Transferring Single-Inductor Bipolar-Output Converter with a Flying Capacitor for Highly Efficient AMOLED Display in 0.5μm CMOS
S-W. Hong, Sookmyung Women’s University, Seoul, Korea

11:45 AM
11.7 A Voltage-Tolerant Three-Level Buck-Boost DC-DC Converter with Continuous Transfer Current and Flying Capacitor Soft Charger Achieving 96.8% Power Efficiency and 0.87μs/V DVS Rate
Samsung Electronics, Hwaseong, Korea

12:00 PM
11.8 A 96.8%-Efficiency Continuous Input/Output-Current Step-Up/Down Converter Powering Disposable IoTs with Reconfigurable Multi-Cell-Balanced Alkaline Batteries
M-W. Ko¹, G-G. Kang¹, K-D. Kim¹, J-H. Lee¹, S. Koh¹, T. Kong², S-H. Kim³, S. Lee², M. Cho², J. Shin², G-H. Cho¹, H-S. Kim¹
¹KAIST, Daejeon, Korea
²Samsung Electronics, Hwaseong, Korea

Conclusion 12:15 PM
Advanced Optical Communication Circuits

Session Chair:
Mounir Meghelli, IBM Thomas J. Watson Research Center, Yorktown Heights, NY
Session Co-Chair: Takashi Takemoto, Hitachi, Sapporo, Japan

8:30 AM

12.1  A 3D-Integrated Microring-Based 112Gb/s PAM-4 Silicon-Photonic Transmitter with Integrated Nonlinear Equalization and Thermal Control
H. Li, G. Balamurugan, M. Sakib, R. Kumar, H. Jayatilleka, H. Rong, J. Jaussi, B. Casper
Intel, Hillsboro, OR

9:00 AM

12.2  A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications
E. Sentieri* 1, T. Copani* 2, A. Paganini 1, M. Traldi 1, A. Palladino 1, A. Santipo 1, L. Gerosa 2, M. Repossi 1, G. Catrini 2, M. Campo 2, F. Radice 1, A. Diodato 1, R. Pelleriti 2, D. Baldi 1, L. Tarantini 1, L. Maggi 1, G. Radaelli 1, S. Cervini 1, F. Clerici 2, A. Moroni 1
*Equally-Credited Authors (ECAs)
1STMicroelectronics, Agrate, Italy
2STMicroelectronics, Catania, Italy

9:30 AM

12.3  A 48GHz BW 225mW/ch Linear Driver IC with Stacked Current-Reuse Architecture in 65nm CMOS for Beyond-400Gb/s Coherent Optical Transmitters
NTT, Kanagawa, Japan

9:45 AM

12.4  A 700mW 4-to-1 SiGe BiCMOS 100GS/s Analog Time-Interleaver
H. Ramon, M. Verplaetse, M. Vanhoecke, H. Li, J. Bauwelincx, P. Ossieur, X. Yin, G. Torts
imec - Ghent University, Ghent, Belgium

Break 10:00 AM
Non-Volatile Memories

Session Chair: Jongmin Park, SK hynix, Icheon, Korea
Session Co-Chair: Yasuhiko Taito, Renesas Electronics, Kodaira, Japan

10:15 AM

13.1 A 1Tb 4b/Cell NAND Flash Memory with $t_{\text{PROG}}=2\text{ms}$, $t_{\text{R}}=110\mu\text{s}$ and 1.2Gb/s High-Speed I/O Rate
Samsung Electronics, Hwaseong, Korea

10:45 AM

13.2 A 1Tb 4b/Cell 96-Stacked-WL 3D NAND Flash Memory with 30MB/s Program Throughput Using Peripheral Circuit Under Memory Cell Array Technique
SK hynix, Icheon, Korea

11:15 AM

13.3 A 22nm 32Mb Embedded STT-MRAM with 10ns Read Speed, 1M Cycle Write Endurance, 10 Years Retention at 150°C and High Immunity to Magnetic Field Interference
TSMC, Hsinchu, Taiwan

11:30 AM

13.4 A 22nm 1Mb 1024b-Read and Near-Memory-Computing Dual-Mode STT-MRAM Macro with 42.6Gb/s Read Bandwidth for Security-Aware Mobile Devices
National Tsing Hua University, Hsinchu, Taiwan

11:45 AM

13.5 A 128Gb 1b/Cell 96-Word-Line-Layer 3D Flash Memory to Improve Random Read Latency with $t_{\text{PROG}}=75\mu\text{s}$ and $t_{\text{R}}=4\mu\text{s}$
1KIOXIA, Yokohama, Japan
2KIOXIA Systems, Yokohama, Japan
3Western Digital, Milpitas, CA

Conclusion 12:15 PM
SESSION 14                       Tuesday February 18th, 1:30 PM

Low-Power Machine Learning
Session Chair: Jun Deguchi, KIOXIA, Kawasaki, Japan
Session Co-Chair: Rangharajan Venkatesan, NVIDIA, Santa Clara, CA

1:30 PM
14.1 A 510nW 0.41V Low-Memory Low-Computation Keyword-Spotting Chip Using Serial FFT-Based MFCC and Binarized Depthwise Separable Convolutional Neural Network in 28nm CMOS
W. Shan¹, M. Yang², J. Xu¹, Y. Lu¹, S. Zhang¹, T. Wang¹, J. Yang¹, L. Shi¹, M. Seok³
¹Southeast University, Jiangsu, China
²EPFL, Neuchâtel, Switzerland
³Columbia University, New York, NY

14.2 A 65nm 24.7μJ/Frame 12.3mW Activation-Similarity-Aware Convolutional Neural Network Video Processor Using Hybrid Precision, Inter-Frame Data Reuse and Mixed-Bit-Width Difference-Frame Data Codec
Z. Yuan¹,², Y. Yang¹, J. Yue¹,², R. Liu¹, X. Feng¹, Z. Lin³, X. Wu³, X. Li¹, H. Yang¹, Y. Liu¹
¹Tsinghua University, Beijing, China
²Pi2star Technology, Beijing, China
³Anhui University, Hefei, China

2:00 PM
J. Yue¹,², Z. Yuan¹,², X. Feng¹, Y. He¹, Z. Zhang³, X. Si³, R. Liu¹, M-F. Chang³, X. Li¹, H. Yang¹, Y. Liu¹
¹Tsinghua University, Beijing, China
²Pi2star Technology, Beijing, China
³National Tsing Hua University, Hsinchu, Taiwan

Break 3:00 PM
SRAM & Compute-In-Memory

Session Chair:
Kyu-Hyoun (KH) Kim, IBM T. J. Watson Research Center, Yorktown Heights, NY
Session Co-Chair: Eric Karl, Intel, Hillsboro, OR

3:15 PM

15.1  A 5nm 135Mb SRAM in EUV and High-Mobility-Channel FinFET Technology with Metal Coupling and Charge-Sharing Write-Assist Circuitry Schemes for High-Density and Low-Vmin Applications
TSMC, Hsinchu, Taiwan

3:45 PM

15.2  A 28nm 64Kb Inference-Training Two-Way Transpose Multibit 6T SRAM Compute-in-Memory Macro for AI Edge Chips
J-W. Su1,2, X. Si1, Y-C. Chou1, T-W. Chang1, W-H. Huang1, Y-N. Tu1, R. Liu1, P-J. Lu1, T-W. Liu1, J-H. Wang1, Z. Zhang1, H. Jiang1, S. Huang1, C-C. Lo1, R-S. Liu1, C-C. Hsieh1, K-T. Tang1, S-S. Sheu1, S-H. Li1, H-Y. Lee2, S-C. Chang2, S. Yu2, M-F. Chang1
1National Tsing Hua University, Hsinchu, Taiwan
2Industrial Technology Research Institute, Hsinchu, Taiwan
3Georgia Institute of Technology, Atlanta, GA

4:15 PM

15.3  A 351TOPS/W and 372.4GOPS Compute-in-Memory SRAM Macro in 7nm FinFET CMOS for Machine-Learning Applications
Q. Dong1, M. E. Sinangil1, B. Erbagci1, D. Sun2, W-S. Khwa2, H-J. Liao2, Y. Wang2, J. Chang2
1TSMC, San Jose, CA
2TSMC, Hsinchu, Taiwan

4:45 PM

15.4  A 22nm 2Mb ReRAM Compute-in-Memory Macro with 121-28TOPS/W for Multibit MAC Computing for Tiny AI Edge Devices
National Tsing Hua University, Hsinchu, Taiwan

5:00 PM

15.5  A 28nm 64Kb 6T SRAM Computing-in-Memory Macro with 8b MAC Operation for AI Edge Chips
X. Si1,2, Y-N. Tu1, W-H. Huang1, J-W. Su1, P-J. Lu1, J-H. Wang1, T-W. Liu1, S-Y. Wu1, R. Liu1, Y-C. Chou1, Z. Zhang1, S-H. Sie1, W-C. Wei1, Y-C. Lo1, T-H. Wen1, T-H. Hsu1, Y-K. Chen1, W. Shih1, C-C. Lo1, R-S. Liu1, C-C. Hsieh1, K-T. Tang1, N-C. Lien1, W-C. Shih1, Y. He2, Q. Li2, M-F. Chang1
1National Tsing Hua University, Hsinchu, Taiwan
2University of Electronic Science and Technology of China, Chengdu, China
3M31 Technology, Hsinchu, Taiwan

Conclusion 5:15 PM
Nyquist & VCO-Based ADCs
Session Chair: Bob Verbruggen, Xilinx, Citywest, Ireland
Session Co-Chair: Takashi Oshima, Hitachi, Tokyo, Japan

1:30 PM
16.1 A 12b 18GS/s RF Sampling ADC with an Integrated Wideband Track-and-Hold Amplifier and Background Calibration
A. M. A. Ali, H. Dinc, P. Bhoraskar, S. Bardsley, C. Dillon, M. Kumar, M. McShea, R. Bunch, J. Prabhakar, S. Puckett
Analog Devices, Greensboro, NC

2:00 PM
16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input
M. Zhang¹, Y. Zhu¹, C-H. Chan¹, R. P. Martins¹²
¹University of Macau, Macau, China
²University of Lisboa, Lisbon, Portugal

2:30 PM
16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation
Z. Zheng¹², L. Wei¹², J. Lagos³, E. Martens³, Y. Zhu¹, C-H. Chan¹, J. Craninckx², R. P. Martins¹³
¹University of Macau, Macau, China
²imec, Leuven, Belgium
³University of Lisboa, Lisbon, Portugal

Break 3:00 PM

3:15 PM
16.4 A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme
T-C. Hung, J-C. Wang, T-H. Kuo, National Cheng Kung University, Tainan, Taiwan

3:45 PM
16.5 A 13b 0.005mm² 40MS/s SAR ADC with kT/C Noise Cancellation
J. Liu¹, X. Tang², W. Zhao², L. Shen², N. Sun²
¹Tsinghua University, Beijing, China
²University of Texas, Austin, TX

4:15 PM
16.6 An 800MHz-BW VCO-Based Continuous-Time Pipelined ADC with Inherent Anti-Aliasing and On-Chip Digital Reconstruction Filter
H. Shibata¹, G. Taylor², B. Schell³, V. Kozlov⁴, S. Patil⁵, D. Paterson⁶, A. Ganesan⁷, Y. Dong⁸, W. Yang⁸, Y. Yin⁸, Z. Li⁸, P. Shrestha⁹, A. Gopa⁹, A. Bhat⁹, S. Pavar⁹
¹Analog Devices, Toronto, Canada
²Analog Devices, San Diego, CA
³Analog Devices, Somerset, NJ
⁴Analog Devices, Wilmington, MA
⁵Analog Devices, Greensboro, NC
⁶Indian Institute of Technology Madras, Chennai, India

4:45 PM
16.7 A 40MHz-BW 76.2dB/78.0dB SNDR/DR Noise-Shaping Nonuniform Sampling ADC with Single Phase-Domain Level Crossing and Embedded Nonuniform Digital Signal Processor in 28nm CMOS
T-F. Wu, M-W. Chen, University of Southern California, Los Angeles, CA

Conclusion 5:15 PM
Frequency Synthesizers & VCOs

Session Chair: Wanghua Wu, Samsung, San Jose, CA
Session Co-Chair: Jiayoon Ru, XINYI Information Technology, Shanghai, China

1:30 PM
17.1 A -240dB-FoM jitter and -115dBc/Hz PN @ 100kHz, 7.7GHz Ring-DCO-Based Digital PLL Using P/I-Gain Co-Optimization and Sequence-Rearranged Optimally Spaced TDC for Flicker-Noise Reduction
Y. Lee*, T. Seong**, J. Lee, C. Hwang†, H. Park, J. Choi‡, *Equally-Credited Authors (ECAs)
*KAIST, Daejeon, Korea; †Ulsan National Institute of Science and Technology, Ulsan, Korea
A. Santiccioli, M. Mercandelli, L. Bertulessi, A. Parisi, D. Cherniak, A. L. Lacaita, C. Samori, S. Levantino
Politecnico di Milano, Milan, Italy; ‡Infineon Technologies, Villach, Austria
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17.3 A -58dBc-Worst-Fractional-Spur and -234dB-FoM jitter, 5.5GHz Ring-DCO-Based Fractional-N DPLL Using a Time-Invariant-Probability Modulator, Generating a Nonlinearity-Robust DTC-Control Word
T. Seong*, Y. Lee*, C. Hwang†, J. Lee, H. Park, K. J. Lee‡, J. Choi§,*Equally-Credited Authors (ECAs)
*KAIST, Daejeon, Korea; †Ulsan National Institute of Science and Technology, Ulsan, Korea
2:45 PM
17.4 A 18.6-to-40.1GHz 201.7dBc/Hz FoM, Multi-Core Oscillator Using E-M Mixed-Coupling Resonance Boosting
Y. Shu, H. J. Qian, X. Luo
University of Electronic Science and Technology of China, Chengdu, China
Break 3:00 PM
3:15 PM
17.5 A 12.5GHz Fractional-N Type-I Sampling PLL Achieving 58fs Integrated Jitter
M. Mercandelli, A. Santiccioli, A. Parisi, L. Bertulessi, D. Cherniak, A. L. Lacaita, C. Samori, S. Levantino
Politecnico di Milano, Milan, Italy; ‡Infineon Technologies, Villach, Austria
3:45 PM
17.6 A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and -250dB FoM
*University College Dublin, Dublin, Ireland; ‡Microelectronic Circuits Centre Ireland, Dublin, Ireland
4:15 PM
17.7 A 12mW 10GHz FMCW PLL Based on an Integrating DAC with 90kHz rms Frequency Error for 23MHz/μs Slope and 1.2GHz Chirp Bandwidth
P. T. Renukaswamy, N. Markulic, S. Park, A. Kankuppe, Q. Shi, P. Wambacq, J. Craninckx
*imec, Leuven, Belgium; †Vrije Universiteit Brussel, Brussels, Belgium
4:45 PM
17.8 A 170MHz-Lock-In-Range and -253dB-FoM jitter, 12-to-14.5GHz Subsampling PLL with a 150μW Frequency-Disturbance-Correcting Loop Using a Low-Power Unevenly Spaced Edge Generator
Y. Lim*, Y. Jo*, J. Kim**, J. Bang†, S. Yoo‡, H. Park, H. Yoon‡, J. Choi§,*Equally-Credited Authors (ECAs), †KAIST, Daejeon, Korea
‡Ulsan National Institute of Science and Technology, Ulsan, Korea
Qualcomm, San Diego, CA
5:00 PM
17.9 A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA
C. Fan, J. Yin, C-C. Lim, P-I. Makii, R. P. Martins
*University of Macau, Macau, China; ‡University of Lisboa, Lisbon, Portugal
Conclusion 5:15 PM
1:30 PM
18.1 A Self-Health-Learning GaN Power Converter Using On-Die Logarithm-Based Analog SGD Supervised Learning and Online $T_J$-Independent Precursor Measurement
Y. Huang, Y. Chen, D. B. Ma, The University of Texas at Dallas, Richardson, TX

2:00 PM
18.2 A Monolithic E-Mode GaN 15W 400V Offline Self-Supplied Hysteretic Buck Converter with 95.6% Efficiency
M. Kaufmann$^1$, M. Lueders$^2$, C. Kaya$^3$, B. Wicht$^4$
$^1$Leibniz University Hannover, Hannover, Germany
$^2$Texas Instruments, Freising, Germany
$^3$Texas Instruments, Dallas, TX

2:30 PM
18.3 A 120mA Non-Isolated Capacitor-Drop AC/DC Power Supply
Y. Ramadass$^{*1}$, A. Blanco$^{*2}$, B. Xiao$^{*3}$, J. Cummings$^3$
$^1$Texas Instruments, Santa Clara, CA
$^2$Texas Instruments, Dallas, TX
$^3$Texas Instruments, Tucson, AZ

2:45 PM
18.4 An 11MHz Fully Integrated 5kV Isolated DC-DC Converter Without Cross-Isolation-Barrier Feedback
L. Li$^1$, X. Fang$^1$, R. Wu$^2$
$^1$CoilEasy Technologies, Chongqing, China
$^2$University of Electronic Science and Technology of China, Chengdu, China

3:00 PM
Break

3:15 PM
18.5 ZVS Flyback-Converter ICs Optimizing USB Power Delivery for Fast-Charging Mobile Devices to Achieve 93.5% Efficiency
W-H. Chang, K-Y. Lin, C-C. Lee, L-D. Lo, J-Y. Lin, T-Y. Yang, Richtek, Hsinchu, Taiwan

3:45 PM
18.6 A 92.8%-Peak-Efficiency 60A 48V-to-1V 3-Level Half-Bridge DC-DC Converter with Balanced Voltage on a Flying Capacitor
M. Choi$^{1,2}$, D-K. Jeong$^1$
$^1$Seoul National University, Seoul, Korea
$^2$Samsung Electronics, Hwaseong, Korea

4:15 PM
18.7 A DC to 35MHz Fully Integrated Single-Power-Supply Isolation Amplifier for Current- and Voltage-Sensing Front-Ends of Power Electronics
S. Takaya, H. Ishihara, K. Onizuka, Toshiba, Kawasaki, Japan

4:45 PM
18.8 A Fully-Generic-Process Galvanic Isolator for Gate Driver with 123mW 23% Power Transfer and Full-Triplex 21/14/0.5Mb/s Bidirectional Communication Utilizing Reference-Free Dual-Modulation FSK
H. Ishihara, K. Onizuka, Toshiba, Kawasaki, Japan

Conclusion 5:15 PM
19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers

B. Patra*, J. P. G. van Dijk*, S. Subramanian*, A. Corna†, X. Xue†, C. Jeon‡, F. Sheikh‡, E. Juarez-Hernandez§, B. Perez Esparza§, H. Rampurawala§, B. Carlton§, N. Samkharadze†, S. Ravikumar†, C. Nieva†, S. Kim‡, H-J. Lee‡, A. Sammak‡, G. Scappucci‡, M. Veldhorst†, L. M. K. Vandersypen†, M. Babaie*†, F. Sebastiano*†, E. Charbon*‡, S. Pellerano*‡
*Equally-Credited Authors (ECAs)
†Delft University of Technology, Delft, The Netherlands
‡Intel, Hillsboro, OR
§Intel, Guadalajara, Mexico
¶TNO, Delft, The Netherlands
5EPFL, Neuchatel, Switzerland

19.2 A 110mK 295 μW 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

L. Le Guevel†, G. Billiot†, X. Jeh‡, S. De Franceschi‡, M. Zurita‡, Y. Thonnart‡, M. Vinet‡, M. Sanquer†, R. Maurand‡, A. G. Jansen‡, G. Pillonnet†
†CEA-LETI-MINATEC, Grenoble, France
‡CEA-IRIG, Grenoble, France

19.3 A 200dB FoM 4-to-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

J. Gong†, Y. Chen†, F. Sebastiano†, E. Charbon‡, M. Babaie†
†Delft University of Technology, Delft, The Netherlands
‡EPFL, Lausanne, Switzerland
§Intel, Hillsboro, OR

Low-Power Circuits for IoT & Health
Session Chair: Nick Van Helleputte, imec, Heverlee, Belgium
Session Co-Chair: Munehiko Nagatani, NTT, Atsugi, Japan

3:15 PM
20.1 A 28 μW IoT Tag That Can Communicate with Commodity WiFi Transceivers via a Single-Side-Band QPSK Backscatter Communication Technique
P-H. P. Wang1,2, C. Zhang1, H. Yang1, D. Bharadia1, P. P. Mercier1
1University of California, San Diego, La Jolla, CA
2Broadcom Inc., San Diego, CA

3:45 PM
Z. Wang1, L. Ye1,2, H. Zhang1, J. Ru1, H. Fan2, Y. Wang1, R. Huang1
1Peking University, Beijing, China
2Advanced Institute of Information Technology of Peking University, Hangzhou, China

4:15 PM
20.3 A 4.0×3.7×1.0mm3-MEMS CMOS Integrated E-Nose with Embedded 4×Gas Sensors, a Temperature Sensor and a Relative Humidity Sensor
S. H. Lee1, K. Park1, J. Lim1, M. Lee1, J. Park1, H. Kim1, Y. O. Lee2, H. S. Ahn2, E. Shin1, H. Ko1, S. Yoo1, H. Ryu1, Y. Park1, J. Kim1, L. Yan1
1Samsung Electronics, Hwaseong, Korea
2Wisol, Osan, Korea

4:45 PM
20.4 3D Surgical Alignment with 100μm Resolution Using Magnetic-Field Gradient-Based Localization
S. Sharma, G. Ding, A. Telikicherla, F. Aghlmand, A. Hashemi Talkhooncheh, M. Wang, M. G. Shapiro, A. Emami
California Institute of Technology, Pasadena, CA

Conclusion 5:15 PM
Demonstration Session 2, Tuesday, February 18th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2020, as noted by the symbol DS2.

7.3 STATICA: A 512-Spin 0.25M-Weight Full-Digital Annealing Processor with a Near-Memory All-Spin-Updates-at-Once Architecture for Combinatorial Optimization with Complete Spin-Spin Interactions

7.4 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparcity Exploitation

9.1 A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4ks/s

12.4 A 700mW 4-to-1 SiGe BiCMOS 100GS/s Analog Time-Interleaver

14.1 A 510nW 0.41V Low-Memory Low-Computation Keyword-Spotting Chip Using Serial FFT-Based MFCC and Binarized Depthwise Separable Convolutional Neural Network in 28nm CMOS

16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input

17.7 A 12mW 10GHz FMCW PLL Based on an Integrating DAC with 90kHz rms Frequency Error for 23MHz/μs Slope and 1.2GHz Chirp Bandwidth

20.4 A 3D Surgical Alignment with 100μm Resolution Using Magnetic-Field Gradient-Based Localization

21.1 A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing

25.3 A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance

26.1 A 4.5mm² Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR Acquisition in Consumer Wearable Devices

26.3 A Closed-Loop Neuromodulation Chipset with 2-Level Classification Achieving 1.5Vp-p CM Interference Tolerance, 35dB Stimulation Artifact Rejection in 0.5ms and 97.8% Sensitivity Seizure Detection


26.5 A 20μW Heartbeat Detection System-on-Chip Powered by Human Body Heat for Self-Sustaining Wearable Healthcare

26.8 A Trimodal Wireless Implantable Neural Interface System-on-a-Chip

26.9 A 0.19×0.17mm² Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry

27.1 A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an 89.1μW Continuous Machine Health Monitoring Wireless Self-Powered System

27.2 MONO: A Performance-Regulated 0.8-to-38MHz DVFS ARM Cortex-M33 SIMD MCU with 10nW Sleep Power

27.3 EM and Power SCA-Resilient AES-256 in 65nm CMOS Through >350× Current-Domain Signature Attenuation

29.1 A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging

29.4 High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

30.8 A 3.5mm×3.8mm Crystal-Less MICS Transceiver Featuring Coverages of ±160ppm Carrier Frequency Offset and 4.8-VSWR Antenna Impedance for Insertable Smart Pills

33.1 A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models

33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing

34.5 Human-Body-Coupled Power-Delivery and Ambient-Energy-Harvesting ICs for a Full-Body-Area Power Sustainability
# TIMETABLE OF ISSCC 2020 SESSIONS

**ISSCC 2020 • SUNDAY FEBRUARY 16TH**

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<td><strong>T1:</strong> Fundamentals of Integrated Transformers</td>
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<td><strong>T2:</strong> Analog Building Blocks of DC-DC Converters</td>
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<td>10:30 AM</td>
<td><strong>T3:</strong> Interface Circuits for Wearable and Implantable Sensing Systems</td>
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<td>1:30 PM</td>
<td><strong>T4:</strong> Basics of Non-Volatile Memories: MRAM, RRAM, and PRAM</td>
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<td>3:30 PM</td>
<td><strong>T5:</strong> Fundamentals of Time-Interleaved ADCs</td>
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<td><strong>T6:</strong> Digital Fractional-N Phase-Locked-Loop Design</td>
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<th>Time</th>
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<tr>
<td>8:00 AM</td>
<td><strong>F1:</strong> Millimeter-Wave 5G: From Soup to Nuts and Bolts</td>
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<td><strong>F2:</strong> How at the Extreme Edge: Machine Learning as the Killer IoT App</td>
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**Evening Events**

<table>
<thead>
<tr>
<th>Time</th>
<th>Events</th>
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<tr>
<td>7:30 PM</td>
<td><strong>EE1:</strong> Student Research Preview: Short Presentations with Poster Session</td>
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<tr>
<td>6:30 PM</td>
<td><strong>EE2a:</strong> “Navigating the Assistant Professorship” (open to the public)</td>
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<tr>
<td>6:30 PM</td>
<td><strong>EE2b:</strong> “Rising to the Top in Industry” (open to the public)</td>
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**Sessions**

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<thead>
<tr>
<th>Time</th>
<th>Session 1: Plenary Session</th>
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<tbody>
<tr>
<td>8:00 PM</td>
<td><strong>EE3:</strong> Industry Showcase</td>
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**ISSCC 2020 • MONDAY FEBRUARY 17TH • PAPER SESSIONS**

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<td>1:30 PM</td>
<td><strong>Session 7:</strong> High-Performance Machine Learning</td>
<td><strong>Session 8:</strong> Highlighted Chip Releases</td>
<td><strong>Session 9:</strong> Noise-Shaping ADCs</td>
<td><strong>Session 10:</strong> High-Performance Transceivers</td>
<td><strong>Session 11:</strong> DC-DC Converters</td>
</tr>
<tr>
<td>12noon to 7:00 PM</td>
<td>Book Displays</td>
<td>Demonstration Session</td>
<td>Author Interviews</td>
<td>Social Hour</td>
<td><strong>Session 12:</strong> Advanced Optical Communication Circuits</td>
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**ISSCC 2020 • TUESDAY FEBRUARY 18TH • PAPER SESSIONS**

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<tr>
<th>Time</th>
<th>Session 7: Advanced Optical Communication Circuits</th>
<th>Session 8: Non-Volatile Memories</th>
<th>Session 9: Nyquist &amp; VCO-Based ADCs</th>
<th>Session 10: Frequency Synthesizers &amp; VCOs</th>
<th>Session 11: GaN &amp; Isolated Power Conversion</th>
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<td>8:30 AM</td>
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<td>1:30 PM</td>
<td><strong>Session 13:</strong> Low-Power Machine Learning</td>
<td><strong>Session 14:</strong> SRAM &amp; Compute-In-Memory</td>
<td><strong>Session 15:</strong> Highlighted Chip Releases</td>
<td><strong>Session 16:</strong> Nyquist &amp; VCO-Based ADCs</td>
<td><strong>Session 17:</strong> Frequency Synthesizers &amp; VCOs</td>
</tr>
<tr>
<td>10:00 AM to 7:00 PM</td>
<td>Book Displays</td>
<td>Demonstration Session</td>
<td>Author Interviews</td>
<td>Social Hour</td>
<td><strong>Session 18:</strong> GaN &amp; Isolated Power Conversion</td>
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**ISSCC 2020 • WEDNESDAY FEBRUARY 19TH • PAPER SESSIONS**

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<tr>
<td>1:30 PM</td>
<td><strong>Session 26:</strong> Biomedical Innovations</td>
<td><strong>Session 27:</strong> IoT &amp; Security</td>
<td><strong>Session 28:</strong> User Interaction &amp; Diagnostic Technologies</td>
<td><strong>Session 29:</strong> Emerging RF &amp; THz Techniques</td>
<td><strong>Session 30:</strong> Efficient Wireless Connectivity</td>
</tr>
<tr>
<td>10:00 AM to 3:00 PM</td>
<td>Book Displays</td>
<td>Demonstration Session</td>
<td>Author Interviews</td>
<td><strong>Session 31:</strong> Digital Circuit Techniques for Emerging Applications</td>
<td><strong>Session 32:</strong> Power Management Techniques</td>
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**ISSCC 2020 • THURSDAY FEBRUARY 20TH**

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<th>Time</th>
<th>Short Course: Circuit Design in Advanced CMOS Technologies — Considerations and Solutions</th>
<th>F3: Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking</th>
<th>F4: Cutting Edge Advances in Electrical and Optical Transceiver Technologies</th>
<th>F5: Power Management as an Enabler of Future SoC’s</th>
<th>F6: Sensors for Health</th>
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<td>8:00 AM</td>
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**Evening Events**

<table>
<thead>
<tr>
<th>Time</th>
<th>Events</th>
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<tbody>
<tr>
<td>8:00 PM</td>
<td><strong>EE3:</strong> Industry Showcase</td>
</tr>
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</table>

**Events Below in Bold Box are Included with your Conference Registration**
EE4: The Smartest Designer in The Universe

Organizers:
Massimo Alioto, National University of Singapore, Singapore
Denis Daly, Omni Design Technologies, US
Tinoosh Mohsenin, University of Maryland, US
Alex Moreno, University of California at Berkeley, US
Mandy Pant, Intel, US
Tim Piessens, Icsense, Belgium
Mahmoud Sawaby, Stanford University, US
Farhana Sheikh, Intel, US
Tom Van Breussegem, Icsense, Belgium

Good silicon engineering is like practicing sports on an Olympic scale. Be the best and be known being the best. But who is actually the smartest designer of the universe? Who is capable of combining endless creativity with superb knowledge and insight? And where will we find this person: in industry or in academia? Or will the students rise up and show the former generation their tail?

In this interactive quiz show, three teams representing industry, academia and students will compete for the honor and the prestigious title: "The Smartest Designer in the Universe". In several rounds, he contestants will solve questions and puzzles covering all parts of electrical engineering.

They will baffle you with their knowledge, surprise your with their wit and entertain you with their to the point remarks. This all topped with a gentle sauce of made of irony, since the smartest designer in the universe should be smart enough to appreciate the special relativity of it all.

Join this session not only to support your own team but enroll in the game. Everybody will be able to actively participate using an app. Show your strength and support your team!

EE5: “Is an Open-Source Hardware Revolution on the Horizon?”

Organizers:
Naveen Verma, Princeton University, Princeton, NJ
Tanay Karnik, Intel, Hillsboro, OR
Kush Gulati, Omni Design Technologies, Milpitas, CA
Sudip Shekhar, UBC, Vancouver, Canada
Rabia Yazicigil, Boston University, Boston, MA

Open-source has revolutionized software, fostering innovation and enhancing productivity. Hardware design is complex in distinct ways, which, on the one hand, makes such progression necessary, but, on the other hand, institutes completely new challenges. Are the challenges show stoppers, or just new ways of thinking and engineering? If open-source hardware could be attained, what would it look like, and would there be significant up-side (e.g., compared to today’s IP licensing)? Whatever the answers, the success of open-source hardware will require alignment, partnership, and collective will across the hardware ecosystem, from design, to methodologies, to business models. This evening session brings together panelists representing and debating from these different perspectives, to make and break the case.

Moderator:
Denis Daly, Omni Design Technologies, Billerica, MA

Panelists:
Rob Aitken, Arm, San Jose, CA
Elad Alon, UCB and Blue Cheetah Analog Design, Berkeley, CA
Bruce Khailany, NVIDIA, Austin, TX
Sailesh Kottapalli, Intel, Hillsboro, OR
Shichin Ouyang, MediaTek, San Jose, CA
David Patterson, UCB and Google, Berkeley and Mountain View, CA
Davide Rossi, UNIBO, Bologna, Italy
Domain-Specific Processors

Session Chair: Massimo Alioto, National University of Singapore, Singapore
Session Co-Chair: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

8:30 AM
21.1 A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing
Y-C. Wu*, Y-L. Chen*, C-H. Yang¹, C-H. Lee², C-Y. Yu³, N-S. Chang¹, L-C. Chen³, J-R. Chang³, C-P. Lin³, H-L. Chen³, C-S. Chen³, J-H. Hung², C-H. Yang¹
*Equally-Credited Authors (ECAs)
¹National Taiwan University, Taipei, Taiwan
²National Chiao Tung University, Hsinchu, Taiwan
³Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan

9:00 AM
21.2 A 1.5μJ/Task Path-Planning Processor for 2D/3D Autonomous Navigation of Micro Robots
C. Chung, C-H. Yang
National Taiwan University, Taipei, Taiwan

9:30 AM
21.3 A 5.69mm² 0.98nJ/Pixel Image-Processing SoC with 24b High-Dynamic-Range and Multiple Sensor Format Support for Automotive Applications
MediaTek, Hsinchu, Taiwan

Break 10:00 AM
22.1 A 1.1V 16GB 640GB/s HBM2E DRAM with a Data-Bus Window-Extension Technique and a Synergistic On-Die ECC Scheme


Samsung Electronics, Hwaseong, Korea

22.2 An 8.5Gb/s/pin 12Gb-LPDDR5 SDRAM with a Hybrid-Bank Architecture using Skew-Tolerant, Low-Power and Speed-Boosting Techniques in a 2nd generation 10nm DRAM Process


Samsung Electronics, Hwaseong, Korea

22.3 A 128Gb 8-High 512GB/s HBM2E DRAM with a Pseudo Quarter Bank Structure, Power Dispersion and an Instruction-Based At-Speed PMBIST


SK hynix, Icheon, Korea

22.4 A 32Gb/s Digital-Intensive Single-Ended PAM-4 Transceiver for High-Speed Memory Interfaces Featuring a 2-Tap Time-Based Decision Feedback Equalizer and an In-Situ Channel-Loss Monitor

P-W. Chiu, C. Kim

University of Minnesota, Minneapolis, MN

22.5 An 8nm 18Gb/s/pin GDDR6 PHY with TX Bandwidth Extension and RX Training Technique


Samsung Electronics, Hwaseong, Korea

22.6 A 0.8-to-2.3GHz Quadrature Error Corrector with Correctable Error Range of 101.6ps Using Minimum Total Delay Tracking and Asynchronous Calibration On-Off Scheme for DRAM Interface

S. Shin1, H-G. Ko1, S. Jang2, D. Kim1, D-K. Jeong1

1Seoul National University, Seoul, Korea
2SK hynix, Icheon, Korea

Conclusion 12:15 PM
Analog Techniques II

Session Chair: Yiannos Manoli, University of Freiburg - IMTEK, Freiburg, Germany
Session Co-Chair: Taeik Kim, Samsung Electronics, Seongnam, Korea

8:30 AM

23.1 A 4GS/s 80dB DR Current-Domain Analog Front-End for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive LiDAR
M. Kashmiri, B. Behroozpour, V. Petkov, K. Wojciechowski, C. Lang
Robert Bosch, Sunnyvale, CA

9:00 AM

23.2 A 70μW 1.19mm² Wireless Sensor with 32 Channels of Resistive and Capacitive Sensors and Edge-Encoded PWM UWB Transceiver
Y. Luo, Y. Li, A. V-Y. Thean, C-H. Heng, National University of Singapore, Singapore

9:30 AM

23.3 A 0-to-60V-Input VCM Coulomb Counter with Signal-Dependent Supply Current and ±0.5% Gain Inaccuracy from -50°C to 125°C
C. van Vroonhoven, Analog Devices, Ismaning, Germany

Break 10:00 AM

10:15 AM

23.4 A 28W -108.9dB/-102.2dB THD/THD+N Hybrid ΔΣ-PWM Class-D Audio Amplifier with 91% Peak Efficiency and Reduced EMI Emission
S. Karmakar 1, H. Zhang 1, R. Van Veldhoven 2, L. Breems 2, M. Berkhourt 3, Q. Fan 1, K.A.A. Makinwa 1
1Delft University of Technology, Delft, The Netherlands
2NXP Semiconductors, Eindhoven, The Netherlands
3NXP Semiconductors, Nijmegen, The Netherlands

10:45 AM

23.5 A 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction
National Cheng Kung University, Tainan, Taiwan

11:15 AM

23.6 A 2pA/√Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous-Time Gain Compensation
E. Kang 1, M. Tan 1, J-S. An 1, Z-Y. Chang 1, P. Vince 2, N. Sénégond 2, T. Mateo 2, C. Meynier 2, M. Pertijs 1
1Delft University of Technology, Delft, The Netherlands
2VERMON, Tours, France

11:45 AM

23.7 A 130dB CMRR Instrumentation Amplifier with Common-Mode Replication
S. Zhang, C. Gao, X. Zhou, Q. Li
University of Electronic Science and Technology of China, Chengdu, China

12:00 PM

23.8 A 41μW 16MS/s 99.2dB-SFDR Capacitively Degenerated Dynamic Amplifier with Nonlinear-Slope-Factor Compensation
Y. Kim 1, 2, S. Park 1, 2, S. Song 1, S. Lee 1, M. Jang 1, C. Lee 1, Y. Chae 1
1Yonsei University, Seoul, Korea
2Samsung Electronics, Hwaseong, Korea

Conclusion 12:15 PM
RF & mm-Wave Power Amplifiers

Session Chair: Swaminathan Sankaran, Texas Instruments, Dallas, TX
Session Co-Chair: Yves Baeyens, Nokia - Bell Labs, Murray Hill, NJ

8:30 AM

24.1 A 24-to-30GHz Watt-Level Broadband Linear Doherty Power Amplifier with Multi-Primary Distributed-Active-Transformer Power-Combining Supporting 5G NR FR2 64-QAM with >19dBm Average \( P_{\text{out}} \) and >19% Average PAE

F. Wang, H. Wang, Georgia Institute of Technology, Atlanta, GA

9:00 AM

24.2 A Reconfigurable Series/Parallel Quadrature-Coupler-Based Doherty PA in CMOS SOI with VSWR Resilient Linearity and Back-Off PAE for 5G MIMO Arrays

N. S. Mannem, M-Y. Huang, T-Y. Huang, S. Li, H. Wang
Georgia Institute of Technology, Atlanta, GA

9:30 AM

24.3 A 28GHz Current-Mode Inverse-Outphasing Transmitter Achieving 40%/31% PA Efficiency at \( P_{\text{sat}}/6\text{dB PBO} \) and Supporting 15Gbit/s 64-QAM for 5G Communication

S. Li, M-Y. Huang, D. Jung, T-Y. Huang, H. Wang
Georgia Institute of Technology, Atlanta, GA

Break 10:00 AM

10:15 AM

24.4 A Watt-Level Multimode Multi-Efficiency-Peak Digital Polar Power Amplifier with Linear Single-Supply Class-G Technique

S-W. Yoo, S-C. Hung, S-M. Yoo, Michigan State University, East Lansing, MI

10:45 AM

24.5 A 15b Quadrature Digital Power Amplifier with Transformer-Based Complex-Domain Power-Efficiency Enhancement

D. Zheng, Y. Yin, Y. Zhu, L. Xiong, Y. Li, N. Yan, H. Xu, Fudan University, Shanghai, China

11:15 AM

24.6 An Instantaneously Broadband Ultra-Compact Highly Linear PA with Compensated Distributed-Balun Output Network Achieving >17.8dBm \( P_{\text{1dB}} \) and >36.6% \( \text{PAE}_{\text{P1dB}} \) over 24 to 40GHz and Continuously Supporting 64-/256-QAM 5G NR Signals over 24 to 42GHz

F. Wang, H. Wang, Georgia Institute of Technology, Atlanta, GA

11:45 AM

24.7 A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS

B. Philippe, P. Reynaert, KU Leuven, Leuven, Belgium

12:00 PM

24.8 A W-Band Power Amplifier with Distributed Common-Source GaN HEMT and 4-Way Wilkinson-Lange Combiner Achieving 6W Output Power and 18% PAE at 95GHz

W. Wang\(^{1,2}\), F. Guo\(^3\), T. Chen\(^2\), K. Wang\(^1\)

\(^{1}\)Tianjin University, Tianjin, China
\(^{2}\)Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing, China

Conclusion 12:15 PM
SESSION 25  
Wednesday February 19th, 8:30 AM

Digital Power Delivery & Clocking Circuits

Session Chair: Keith Bowman, Qualcomm, Raleigh, NC
Session Co-Chair: Yvain Thonnart, CEA-Leti, Grenoble, France

8:30 AM
25.1 A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS
S. Bang, W. Lim, C. Augustine, A. Malavasi, M. Khellah, J. Tschanz, V. De
Intel, Hillsboro, OR

9:00 AM
25.2 A 480mA Output-Capacitor-Free Synthesizable Digital LDO Using CMP-Triggered Oscillator and Droop Detector with 99.99% Current Efficiency, 1.3ns Response Time, and 9.8A/mm² Current Density
J. Oh, J-E. Park, Y-H. Hwang, D-K. Jeong, Seoul National University, Seoul, Korea

9:30 AM
25.3 A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance
Y. He, K. Yang, Rice University, Houston, TX

9:45 AM
25.4 A Scalable 20GHz On-Die Power-Supply Noise Analyzer with Compressed Sensing
P. Zhai, X. Zhou, Y. Cai, Z. Zhu, F. Zhang, Q. Li
University of Electronic Science and Technology of China, Chengdu, China

Break 10:00 AM

10:15 AM
25.5 A Self-Calibrated 1.2-to-3.8GHz 0.0052mm² Synthesized Fractional-N MDLL Using a 2b Time-Period Comparator in 22nm FinFET CMOS
S. Kundu, L. Chai, K. Chandrashekar, S. Pellerano, B. Carlton, Intel, Hillsboro, OR

10:45 AM
25.6 A 5.25GHz Subsampling PLL with a VCO-Phase-Noise Suppression Technique
H-H. Ting, T-C. Lee, National Taiwan University, Taipei, Taiwan

11:00 AM
25.7 Time-Borrowing Fast Mux-D Scan Flip-Flop with On-Chip Timing/Power/V<sub>MIN</sub> Characterization Circuits in 10nm CMOS
A. Agarwal¹, S. Hsu², S. Realloc⁴, M. Anders¹, G. Chen¹, M. Kar¹, R. Kumar¹, H. Sumbul⁶, P. Knag¹, H. Kaul¹, S. Mathew¹, M. Kumashikara³, R. Krishnamurthy¹, V. De¹
¹Intel, Hillsboro, OR; ²Intel, Bangalore, India

11:15 AM
25.8 A Near-Threshold-Voltage Network-on-Chip with a Metastability Error Detection and Correction Technique for Supporting a Quad-Voltage/Frequency-Domain Ultra-Low-Power System-on-a-Chip
C. Lin¹, W. He¹, Y. Sun¹, B. Pei¹, Z. Mao¹, M. Seok²
¹Shanghai Jiao Tong University, Shanghai, China; ²Columbia University, New York, NY

11:45 AM
25.9 Reconfigurable Transient Current-Mode Global Interconnect Circuits in 10nm CMOS for High-Performance Processors with Wide Voltage-Frequency Operating Range
Intel, Hillsboro, OR

Conclusion 12:15 PM
Biomedical Innovations

Session Chair: Jerald Yoo, National University of Singapore, Singapore
Session Co-Chair: Esther Rodriguez-Villegas, Imperial College London, London, United Kingdom

8:30 AM

26.1 A 4.5mm² Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR

Acquisition in Consumer Wearable Devices


9:00 AM

26.2 A Neuromorphic Multiplier-Less Bit-Serial Weight-Memory-Optimized 1024-Tree Brain-State Classifier and Neuromodulation SoC with an 8-Channel Noise-Shaping SAR ADC Array

G. O’Leary1, J. Xu1, L. Long1, J. Sales Filho1, C. Tejiero1, M. ElAnsary1, C. Tang1, H. Moradì2, P. Shah1, T.A. Valiante3, R. Genov4
1University of Toronto, Toronto, Canada; 2Krembil Neuroscience Center, Toronto, ON, Canada
3Toronto Western Hospital, Toronto, Canada

9:30 AM

26.3 A Closed-Loop Neuromodulation Chipset with 2-Level Classification Achieving 1.5Vpp CM Interference Tolerance, 35dB Stimulation Artifact Rejection in 0.5ms and 97.8% Sensitivity Seizure Detection

Y. Wang1, Q. Sun1, H. Luo1, X. Chen2, X. Wang2, H. Zhang1
1Xi’an Jiaotong University, Xi’an, China; 2Hangzhou Nuowei Medical Technology, Hangzhou, China
3Xi’an Aerosemi Technology, Xi’an, China

Break 10:00 AM

10:15 AM


J-C. Chien, H. T. Soh, A. Arbabian, Stanford University, Stanford, CA

10:30 AM

26.5 A 20µW Heartbeat Detection System-on-Chip Powered by Human Body Heat for Self-Sustaining Wearable Healthcare

S. Bose*, B. Shen*, M. L. Johnston, *Equally-Credited Authors (ECAs), Oregon State University, Corvallis, OR

10:45 AM

26.6 A 6.5µW 10kHz-BW 80.4dB-SNDR Continuous-Time ΔΣ Modulator with Gm-Input and 300mV pp Linear Input Range for Closed-Loop Neural Recording

C. Lee1, T. Jeon1, M. Jang1, S. Park2, Y. Huh2, Y. Chae2
1Yonsei University, Seoul, Korea; 2University of Science and Technology, Daejeon, Korea
3Catholic Kwandong University, Incheon, Korea

11:15 AM

26.7 A 280µW 108dB DR Readout IC with Wireless Capacitive Powering Using a Dual-Output Regulating Rectifier for Implantable PPG Recording

F. Marefat, R. Erfani, K. L. Kilgore, P. Mohseni, Case Western Reserve University, Cleveland, OH

11:45 AM

26.8 A Trimodal Wireless Implantable Neural Interface System-on-a-Chip

Y. Jia1, U. Guler1, Y-P. Lai2, Y. Gong3, A. Weber3, W. Li4, M. Ghovanloo5
1North Carolina State University, Raleigh, NC; 2WPI, Worcester, MA
3Georgia Institute of Technology, Atlanta, GA; 4Michigan State University, East Lansing, MI
5Bionic Sciences, Atlanta, GA

12:00 PM

26.9 A 0.19×0.17mm² Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry

J. Lim1, E. Moon1, M. Barrow1, S. R. Nason1, P. R. Patel1, P. G. Patil1, S. Oh1, I. Lee1, H-S. Kim1, D. Sylvester1, D. Blaauw1, C. A. Chestek1, J. Phillips1, T. Jang2
1University of Michigan, Ann Arbor, MI; 2ETH Zürich, Zürich, Switzerland

Conclusion 12:15 PM
IoT & Security

Session Chair: Hirofumi Shinohara, Waseda University, Fukuoka, Japan
Session Co-Chair: James Myers, Arm, Cambridge, United Kingdom

1:30 PM

27.1 A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an 89.1µW Continuous Machine Health Monitoring Wireless Self-Powered System

J. K. Brown¹, D. Abdallah², J. Boley³, N. Collins¹, K. Craig³, G. Glennon², K-K. Huang³, C. J. Lukas³, W. Moore⁴, R. K. Sawyer³, Y. Shakhsheer²,⁴, F. B. Yahya², A. Wang³, N. E. Roberts⁵, D. D. Wentzloff⁶, B. H. Calhoun²

¹Everactive, Ann Arbor, MI
²Everactive, Charlottesville, VA
³Everactive, Santa Clara, CA
⁴now with Analog Devices, Fort Collins, CO

2:00 PM

27.2 MONO: A Performance-Regulated 0.8-to-38MHz DVFS ARM Cortex-M33 SIMD MCU with 10nW Sleep Power

P. Prabhat¹, B. Labbe¹, G. Knight¹, A. Savanth¹, J. Svedas¹, M. J. Walker¹, S. Jeloka¹, P. M.-Y. Fan¹, F. García-Redondo¹, T. Achuthan¹, J. Myers¹

¹ARM, Cambridge, United Kingdom
²ARM, Austin, TX

2:15 PM

27.3 EM and Power SCA-Resilient AES-256 in 65nm CMOS Through >350× Current-Domain Signature Attenuation

D. Das¹, J. Danial¹, A. Golder², N. Modak¹, S. Maity¹, B. Chatterjee¹, D. Seo¹, M. Chang², A. Varna³, H. Krishnamurthy³, S. Mathew³, S. Ghosh³, A. Raychowdhury³, S. Sen⁴

¹Purdue University, West Lafayette, IN
²Georgia Institute of Technology, Atlanta, GA
³Intel, Chandler, AZ
⁴Intel Labs, Portland, OR

2:30 PM

27.4 Physically Uncloneable Function in 28nm FDSOI Technology Achieving High Reliability for AEC-Q100 Grade 1 and ISO26262 ASIL-B


Samsung Electronics, Hwaseong, Korea

Break 3:00 PM
User Interaction & Diagnostic Technologies
Session Chair: Masayuki Miyamoto, Wacom, Shinjuku, Japan
Session Co-Chair: Johan Vanderhaegen, Google, Mountain View, CA

3:15 PM

28.1 A Capacitive Touch Chipset with 33.9dB Charge-Overflow Reduction Using Amplitude-Modulated Multi-Frequency Excitation and Wireless Power and Data Transfer to an Active Stylus
J-S. An¹, J-H. Ra², E. Kang¹, M. A. P. Pertijs¹, S-H. Han³
¹Delft University of Technology, Delft, The Netherlands
²SK hynix, Icheon, Korea
³Leading UI, Anyang, Korea

3:30 PM

28.2 A 51dB-SNR 120Hz-Scan-Rate 32×18 Segmented-VCOM LCD In-Cell Touch-Display- Driver IC with 96-Channel Compact Shunt-Sensing Self-Capacitance Analog Front-End
H. Jang, H. Shin, J. Lee, C. Yoo, K. Chun, I. Yun
Sentron, Daejeon, Korea

4:00 PM

28.3 A 5.2Mpixel 88.4dB-DR 12in CMOS X-Ray Detector with 16b Column-Parallel Continuous-Time ΔΣ ADCs
S. Lee¹, J. Jeong², T. Kim¹, C. Park¹, T. Kim², Y. Chae¹
¹Yonsei University, Seoul, Korea
²Rayence, Hwaseong, Korea

4:30 PM

28.4 A CMOS Multimodality In-Pixel Electrochemical and Impedance Cellular Sensing Array for Massively Paralleled Synthetic Exoelectrogen Characterization
D. Jung¹, S. R. Kumashi¹, J. Park², S. T. Sanz², S. Grijalva², A. Wang¹, S. Li³, H. C. Cho⁴, C. Ajo-Franklin⁵, H. Wang¹
¹Georgia Institute of Technology, Atlanta, GA
²Intel, Hillsboro, OR
³Lawrence Berkeley National Laboratory, Berkeley, CA
⁴Emory University, Atlanta, GA
⁵Rice University, Houston, TX

Conclusion 4:45 PM
Emerging RF & THz Techniques
Session Chair: Hua Wang, Georgia Institute of Technology, Atlanta, GA
Session Co-Chair: Shuhei Amakawa, Hiroshima University, Hiroshima, Japan

1:30 PM
29.1 A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging
R. Jain, P. Hillger, J. Grzyb, U. R. Pfeiffer, University of Wuppertal, Wuppertal, Germany

2:00 PM
29.2 A 0.59THz Beam-Steerable Coherent Radiator Array with 1mW Radiated Power and 24.1dBm EIRP in 40nm CMOS
K. Guo, P. Reynaert, KU Leuven, Leuven, Belgium

2:30 PM
29.3 Non-Magnetic 0.18 μm SOI Circulator with Multi-Watt Power Handling Based on Switched-Capacitor Clock Boosting
A. Nagulu, T. Chen, G. Zussman, H. Krishnaswamy
Columbia University, New York, NY

2:45 PM
29.4 High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance
M. Khorshidian*, N. Reiskarimian*, H. Krishnaswamy1
*Equally-Credited Authors (ECAs), 1Columbia University, New York, NY

Break 3:00 PM
3:15 PM
29.5 Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers
C. Wang, X. Yi, M. Kim, R. Han
Massachusetts Institute of Technology, Cambridge, MA

3:45 PM
29.6 A 660-to-676GHz 4×2 Oscillator-Radiator Array with Intrinsic Frequency-Filtering Feedback for Harmonic Power Boost Achieving 7.4dBm EIRP in 40nm CMOS
G. Guimaraes, P. Reynaert, KU Leuven, Leuven, Belgium

4:15 PM
29.7 A 490GHz 32mW Fully Integrated CMOS Receiver Adopting Dual-Locking FLL
K-S. Choi1, D. R. Utomo1, K-M. Kim1, B-H. Yun1, S-G. Lee1, I-Y. Lee2
1KAIST, Daejeon, Korea; 2Chosun University, Gwangju, Korea

4:45 PM
29.8 THzID: A 1.6mm2 Package-Less Cryptographic Identification Tag with Backscattering and Beam-Steering at 260GHz
M. I. Ibrahim1, M. I. W. Khan1, C. S. Juvekar1, W. Jung2, R. T. Yazicigil3, A. P. Chandrakasan1, R. Han1
1Massachusetts Institute of Technology, Cambridge, MA; 2Analog Devices, Boston, MA; 3Boston University, Boston, MA

5:00 PM
29.9 A 4×4 Distributed Multi-Layer Oscillator Network for Harmonic Injection and THz Beamforming with 14dBm EIRP at 416GHz in a Lensless 65nm CMOS IC
Princeton University, Princeton, NJ

Conclusion 5:15 PM
Efficient Wireless Connectivity

Session Chair: Yao-Hong Liu, imec-Netherlands, Eindhoven, The Netherlands
Session Co-Chair: Yuu Watanabe, Waseda University, Atsugi, Japan

1:30 PM
30.1 A Temperature-Robust 27.6nW -65dBm Wakeup Receiver at 9.6GHz X-Band
P. Bassirian, D. Duvvuri, D. S. Truesdell, N. Liu, B. H. Calhoun, S. M. Bowers
University of Virginia, Charlottesville, VA

2:00 PM
30.2 NB-IoT and GNSS All-in-One System-on-Chip Integrating RF Transceiver, 23dBm CMOS Power Amplifier, Power Management Unit and Clock Management System for Low-Cost Solution
J. Lee, J. Han, C. Lo, J. Lee, W. Kim, S. Kim, B. Kang, J. Han, S. Jung, T. Nomiyama, J. Lee, T. B. Cho, I. Kang, Samsung Electronics, Hwaseong, Korea

2:30 PM
30.3 A SAW-Less NB-IoT RF Transceiver with Hybrid Polar and On-Chip Switching PA Supporting Power Class 3 Multi-Tone Transmission
Hong Kong Applied Science and Technology Research Institute, Hong Kong, China

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30.4 A 370µW 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-Compliant Receiver with >63dB Adjacent Channel Rejection at >2 Channels Offset in 22nm FDSOI
B. J. Thijssen1, E. A. M. Klumperink1, P. Quinlan2, B. Nauta1
1University of Twente, Enschede, The Netherlands; 2Analog Devices, Cork, Ireland

3:30 PM
30.5 A 0.5V BLE Transceiver with a 1.9mW RX Achieving -96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI
M. Tamura1, H. Takano1, S. Shinke1, H. Fujita1, H. Nakahara1, N. Suzuki1, Y. Nakada2, Y. Shinohe2, S. Etou1, T. Fujiwara2, Y. Katayama2
1Sony Semiconductor Solutions, Atsugi, Japan; 2Sony LSI Design, Atsugi, Japan

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30.6 A Low-Power BLE Transceiver with Support for Phase-Based Ranging, Featuring 5µs PLL Locking Time and 5.3ms Ranging Time, Enabled by Staircase-Chirp PLL with Sticky-Lock Channel-Switching
E. Bechthum1, J. Dijkhuis1, M. Ding1, Y. He1, J. Van den Heuvel1, P. Mateman1, G-J. van Schaik1, K. Shibata2, M. Song1, E. Tiurin1, S. Traferro1, Y-H. Liu1, C. Bachmann1
1imec-Netherlands, Eindhoven, The Netherlands; 2Renesas Electronics, Tokio, Japan

4:30 PM
30.7 A Crystal-Less BLE Transmitter with -86dBm Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet
A. Alghaihab1, X. Chen1, Y. Shi1, D. S. Truesdell1, B. H. Calhoun2, D. D. Wentzloff1
1University of Michigan, Ann Arbor, MI; 2University of Virginia, Charlottesville, VA

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30.8 A 3.5mm×3.8mm Crystal-Less MICS Transceiver Featuring Coverages of ±160ppm Carrier Frequency Offset and 4.8-VSWR Antenna Impedance for Insertable Smart Pills
M. Song1, M. Ding1, E. Tiurin1, K. Xu1, E. Allebè1, G. Singh1, P. Zhang1, S. Traferro1, H. Korpela1, N. van Helleputte1, R. B. Staszewski2, Y-H. Liu1, C. Bachmann1
1imec-Netherlands, Eindhoven, The Netherlands; 2University College Dublin, Dublin, Ireland

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Conclusion 5:15 PM
Digital Circuit Techniques for Emerging Applications

Session Chair: Alicia Klinefelter, Nvidia, Durham, NC
Session Co-Chair: Mijung Nah, Samsung Electronics, Yong-in, Korea

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31.1 A 65nm 8.79TOPS/W 23.82mW Mixed-Signal Oscillator-Based NeuroSLAM Accelerator for Applications in Edge Robotics
J-H. Yoon, A. Raychowdhury
Georgia Institute of Technology, Atlanta, GA

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31.2 CIM-Spin: A 0.5-to-1.2V Scalable Annealing Processor Using Digital Compute-In-Memory Spin Operators and Register-Based Spins for Combinatorial Optimization Problems
Y. Su*, H. Kim*, B. Kim
*Equally-Credited Authors (ECAs)
Nanyang Technological University, Singapore

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31.3 A Compute-Adaptive Elastic Clock-Chain Technique with Dynamic Timing Enhancement for 2D PE-Array-Based Accelerators
T. Jia, Y. Ju, J. Gu
Northwestern University, Evanston, IL

Break 3:00 PM
Power Management Techniques

Session Chair: Chanhong Chern, TSMC, Hsinchu, Taiwan
Session Co-Chair: Li Geng, Xi’an Jiaotong University, Xi’an, China

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32.1 A 13.56MHz Current-Mode Wireless Power and Data Receiver with Efficient Power Extracting Controller and Energy-Shift Keying Technique for Loosely Coupled Implantable Devices
S-W. Hong
Sookmyung Women’s University, Seoul, Korea

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32.2 Self-Tunable Phase-Shifted SECE Piezoelectric Energy-Harvesting IC with a 30nW MPPT Achieving 446% Energy-Bandwidth Improvement and 94% Efficiency
A. Morel¹, A. Quelen¹, C. A. Berlitz¹, D. Gibus¹, P. Gasnier¹, A. Badel², G. Pillonnet¹
¹CEA-LETI-MINATEC, Grenoble, France
²Université Savoie-Mont Blanc, Annecy, France

4:15 PM

32.3 Electromagnetic Mechanical Energy-Harvester IC with No Off-Chip Component and One Switching Period MPPT Achieving up to 95.9% End-to-End Efficiency and 460% Energy-Extraction Gain
A. Quelen, G. Pillonnet, P. Gasnier, F. Rummens, S. Boisseau
CEA-LETI-MINATEC, Grenoble, France

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32.4 A 0.4-to-1.2V 0.0057mm² 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement
J-E. Park, J. Hwang, J. Oh, D-K. Jeong
Seoul National University, Seoul, Korea

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32.5 A Scalable and PCB-Friendly Daisy-Chain Approach to Parallelize LDO Regulators with 2.613% Current-Sharing Accuracy Using Dynamic Element Matching for Integrated Current Sensing
B. Talele¹, R. Magod², K. Kunz³, S. Manandhar², B. Bakkaloglu¹
¹Arizona State University, Tempe, AZ
²Texas Instruments, Dallas, TX
³Texas Instruments, Tucson, AZ

Conclusion 5:15 PM
Non-Volatile Devices for Future Architecture

Session Chair: Munehiko Nagatani, NTT, Atsugi, Japan
Session Co-Chair: Nick Van Helleputte, imec, Heverlee, Belgium

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33.1 A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models

W. Wan¹, R. Kubendran², S. B. Eryilmaz¹, W. Zhang³, Y. Liao⁴, D. Wu⁵, S. Deiss², B. Gao³, P. Raina¹, S. Joshi², H. Wu⁵, G. Cauwenberghs², H-S. P. Wong¹
¹Stanford University, Stanford, CA
²University of California, San Diego, CA
³Tsinghua University, Beijing, China
⁴University of Notre Dame, Notre Dame, IN

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33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing

Q. Liu¹, B. Gao¹, P. Yao¹, D. Wu¹, J. Chen¹, Y. Pang¹, W. Zhang¹, Y. Liao¹, C-X. Xue², W-H. Chen², J. Tang¹, Y. Wang¹, M-F. Chang², H. Qian¹, H. Wu¹
¹Tsinghua University, Beijing, China
²National Tsing Hua University, Hsinchu, Taiwan

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33.3 Via-Switch FPGA: 65nm CMOS Implementation and Architecture Extension for AI Applications

M. Hashimoto¹, X. Bai², N. Banno², M. Tada², T. Sakamoto², J. Yu¹, R. Doi¹, Y. Araki³, H. Onodera², T. Imagawa¹, H. Ochi², K. Wakabayashi², Y. Mitsuyama², T. Sugibayashi²
¹Osaka University, Suita, Japan
²NEC, Tsukuba, Japan
³Kyoto University, Kyoto, Japan
⁴Ritsumeikan University, Kusatsu, Japan
⁵NEC, Kawasaki, Japan
⁶Kochi University of Technology, Kami, Japan

Break 3:00 PM
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34.1 A 64×64 Implantable Real-Time Single-Charged-Particle Radiation Detector for Cancer Therapy

K. Lee¹, J. Scholey², E. B. Norman¹, I. K. Daftari², K. K. Mishra², B. A. Faddegon², M. M. Maharbiz¹, M. Anwar²
¹University of California, Berkeley, CA
²University of California, San Francisco, CA

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34.2 1225-Channel Localized Temperature-Regulated Neuromorphic Retinal-Prosthesis SoC with 56.3nW/Channel Image Processor

J. H. Park¹, J. S. Y. Tan¹, H. Wu¹, J. Yoo¹,²
¹National University of Singapore, Singapore
²N.1 Institute for Health, Singapore

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34.3 An 8.2mm³ Implantable Neurostimulator with Magnetoelectric Power and Data Transfer

*Equally-Credited Authors (ECAs)
Rice University, Houston, TX

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34.4 A 4.5mm³ Deep-Tissue Ultrasonic Implantable Luminescence Oxygen Sensor

S. Sonmezoglu, M. M. Maharbiz
University of California, Berkeley, CA

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34.5 Human-Body-Coupled Power-Delivery and Ambient-Energy-Harvesting ICs for a Full-Body-Area Power Sustainability

J. Li¹, Y. Dong¹, J. H. Park¹, L. Lin¹, T. Tang¹, M. Zhang¹, H. Wu¹, L. Zhang¹, J. S. Y. Tan¹, J. Yoo¹,²
*Equally-Credited Authors (ECAs)
¹National University of Singapore, Singapore
²N.1 Institute for Health, Singapore

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34.6 EEG Dust: A BCC-Based Wireless Concurrent Recording/Transmitting Concentric Electrode

T. Tang¹, L. Yan², J. H. Park¹, H. Wu¹, L. Zhang¹, H. Y. B. Lee¹, J. Yoo¹,³
¹National University of Singapore, Singapore
²Samsung Electronics, Suwon, Korea
³N.1 Institute for Health, Singapore

Conclusion 5:15 PM
Short Course:  
**Circuit Design in Advanced CMOS Technologies — Considerations and Solutions**

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**Topic:**  
Breakfast  
Introduction by Chair, **Daniel Friedman**  
*IBM Thomas J. Watson Research Center, Yorktown Heights, NY*  
Device and Physical Design Considerations for Circuits in FinFET Technology  
**Alvin Leng Sun Loke**, TSMC, San Diego, CA  
Break  
Modeling and RF Design Considerations for Advanced CMOS Technology  
**Ali M. Niknejad**, University of California at Berkeley, Berkeley, CA  
Lunch  
High-Speed and Mixed-Signal Circuit Design Techniques in FinFET Technology for Wireline and Optical Interface Applications  
**Jonathan E. Proesel**, IBM T. J. Watson Research Center, Yorktown Heights, NY  
Break  
Embedded Memory and Support-Circuitry Design Considerations in Advanced CMOS Technology  
**Eric Karl**, Intel, Portland, OR  
Conclusion

**Introduction**

Technology scaling in CMOS has brought with it an ever-growing set of constraints and challenges that must be faced not only by the technologist but also by the circuit designer. Understanding the restrictions imposed by the technology and incorporating strategies to achieve design goals in light of those restrictions are both critical to successful development of state-of-the-art CMOS integrated circuits in advanced nodes, especially those using FinFET devices. In this short course, the first presentation will provide a framework for understanding physical design constraints and physical design approaches in the context of FinFET technology and how such constraints will influence circuit design. The second presentation will discuss approaches to RF circuit design in the context of advanced CMOS nodes. The third presentation will cover the design of critical mixed-signal circuits in FinFET technology, including high-speed I/O building blocks and optical interface circuits. Finally, the fourth presentation will cover the design of embedded memory elements in advanced node technology, focusing on SRAM and associated support circuitry.
SC1: Device and Physical Design Considerations for Circuits in FinFET Technology

Alvin Leng Sun Loke, TSMC, San Diego, CA

CMOS scaling remains economically lucrative with 7nm mobile SoCs commercialized since late 2018 and 5nm products imminently available. Modest feature-size reduction and process innovations optimized for logic and SRAM scaling continue to offer compelling node-to-node power, performance, area, and cost benefits. This talk provides an overview of the key process technology elements that have enabled the FinFET CMOS nodes and highlights the resulting technology impact on design.

Alvin Loke is a Director in the TSMC San Diego Design Center focusing on analog design methodologies and technology co-optimization in advanced CMOS. He received his PhD from Stanford in 1999, spent several years in CMOS process integration, and worked on wireline/clocking design and design/technology interface at Agilent, AMD, and Qualcomm. Alvin has authored over 50 publications and 28 patents. He is currently a VLSI Symposia TPC member, SSCS Webinar Coordinator for North America, and San Diego SSCS Chapter Chair. He previously served as a Distinguished Lecturer, CICC TPC member, and JSSC and SSCL Guest Editor. Alvin is recipient of the Canadian NSERC 1967 Scholarship, 2005 SSCS Outstanding Chapter Award, and CICC 2018 Best Paper Award.

SC2: Modeling and RF Design Considerations for Advanced CMOS Technology

Ali M. Niknejad, University of California at Berkeley, Berkeley, CA

Advanced CMOS technology nodes are extremely complex marvels of engineering, offering nanoscale devices and metallization approaching terahertz speeds. In this tutorial, we will consider fundamental transistor and circuit properties such as gain, bandwidth, noise, and distortion. We will discuss how circuit design is impacted by advanced technology parameters and how to model these effects to design robust RF circuits.

Ali M. Niknejad received the Ph.D. degree in electrical engineering from the University of California, Berkeley. He holds the Donald O. Pederson Distinguished Professorship chair in the EECS department at UC Berkeley and is a faculty co-director of the Berkeley Wireless Research Center (BWRC). He is also the Associate Director of the Center for Converged TeraHertz Communications and Sensing (ComSenTer). Professor Niknejad is the recipient the 2017 IEEE Transactions on Circuits and Systems Darlington Best Paper Award, the 2017 Most Frequently Cited Paper Award (2010 to 2016) from the Symposium on Very Large-Scale Integration Circuits, the CICC 2015 Best Invited Paper Award, and the 2012 ASEE Frederick Emmons Terman Award.
SC3: High-Speed and Mixed-Signal Circuit Design Techniques in FinFET Technology for Wireline and Optical Interface Applications

Jonathan E. Proesel, IBM T. J. Watson Research Center, Yorktown Heights, NY

Getting the best possible performance from analog and mixed-signal circuits requires a strong understanding of the underlying IC technology. Advanced FinFET CMOS technologies have the potential for excellent analog and mixed-signal performance. However, these technologies have many pitfalls for the unwary designer: highly restrictive design rules, thin metal layers, and device self-heating, to name a few problems. This talk explores how to capture the benefits and avoid the problems of FinFET technology in high-speed wireline communications circuits. The talk begins with a brief introduction to wireline communications circuits. Then it discusses FinFET technology and the impact to high-speed wireline circuits. A set of example circuit designs in 14nm FinFET are reviewed, studying system, circuit, and layout details. Finally, the talk concludes with a set of tips and techniques to get the most out of FinFET technologies.

Jonathan Proesel is a Research Staff Member at IBM T. J. Watson Research Center, where he has conducted circuit design research since 2010. He has designed analog and mixed-signal circuits in many silicon technologies, such as 130nm SiGe BiCMOS, 90nm SOI CMOS with monolithically integrated Si photonics, and 14 and 7nm FinFET. His primary research focus is high-speed optical and electrical wireline communications, and his other interests include silicon photonics, data converters, AI hardware, and design-technology co-optimization. He received the Ph.D. degree from Carnegie Mellon University in 2010. He is a co-recipient of the 2010 IEEE CICC Best Student Paper Award and the 2018 IEEE Photonics Technology Journal Best Paper Award. At IBM, he has received multiple technical awards. He serves on the technical program committee for the Symposium on VLSI Circuits.

SC4: Embedded Memory and Support-Circuitry Design Considerations in Advanced CMOS Technology

Eric Karl, Intel, Portland, OR

Rapidly accelerating compute requirements are driving the need for improved bandwidth, reduced latency, higher density and better energy efficiency from the memory hierarchy. Embedded memories play a critical role in mitigating the latency and bandwidth limitations of accessing external, storage-class memories. This course will explore the challenges of embedded SRAM, DRAM, MRAM and RRAM in advanced technologies and focus on state-of-the-art-circuit techniques used to assist memory functionality and performance.

Eric Karl (S’03–M’08) received B.S.E., M.S.E. and Ph.D. degrees in Electrical Engineering from the University of Michigan, Ann Arbor, Michigan in 2002, 2004 and 2008, respectively. Dr. Karl held positions at Intel Circuit Research Lab, IBM T.J. Watson Research Center and Sun Microsystems prior to 2008. In 2008, he joined Intel Logic Technology Development, where he is a Senior Principal Engineer engaged in the development of memory circuit technology for low-power and high-performance SoC applications. Dr. Karl has published 27 conference papers and technical journal articles.
Custom processors are becoming more ubiquitous in the Machine Learning (ML) space, but motivating their design through informed application constraints has been challenging in this emerging and rapidly evolving area. Additionally, ML processors range from pure inference devices to general purpose processors with training capabilities and should not be designed at the hardware level in isolation. This forum looks across the HW and SW stacks to focus on 1) analyzing key ML applications, 2) which inference, but also training algorithms are of interest; 3) how custom designed ML processor architectures are driven by applications and algorithms, 4) how ML processors can be benchmarked on applications that matter. As such, the forum gives audience insights on effective ML processor development by shedding light on applications, algorithms, architectures, benchmarking, and time to market perspectives.

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<td>Evolution of DNN Accelerators: From Big Cloud to Small Mobile Deep Learning</td>
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<td>Global-Scale FPGA-Accelerated DNN Inference</td>
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<td>Heterogeneous Computing Platforms for Autonomous Vehicles</td>
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<td>The Vision Behind MLPerf: A Community-Driven ML Benchmark Suite for Software Frameworks and Hardware Accelerators in Cloud and Edge Computing</td>
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<td>4:00 PM</td>
<td>Panel Discussion: How Should ML Processors be Benchmarked on Applications That Matter?</td>
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F4: Cutting Edge Advances in Electrical and Optical Transceiver Technologies

Organizers: Thomas Toifl, Cisco Systems, Zurich, Switzerland
Munehiko Nagatani, NTT, Atsugi, Kanagawa, Japan

Committee: Andrew Joy, Marvell, Irvine, CA
Frederic Giansello, STMicroelectronics, Crolles, France
Mounir Meghelli, IBM, Yorktown Heights, NY
Sudip Shekhar, University of British Columbia, Vancouver, Canada

This forum reviews current state of the art and future prospects of wireline interfaces and electronic-photonic integration technologies for ultrahigh-speed links.

Electrical interface speeds are reaching 112Gb/s but are now facing severe limitations due to channel bandwidth, power consumption and circuit complexity. The first part of the forum discusses standards, modulation formats, signaling and circuit techniques of state-of-the-art transceivers and how to potentially overcome these limitations above 112Gb/s.

With increasing demand on bandwidth, optical links are constantly expanding into new territory. The second part of the forum will review electronic-photonic integrated subsystems, which are now commercially produced in high volumes. In particular, silicon photonics technologies, including foundry services, design tools, and packaging, have matured rapidly in the past few years. Also, enabled by electronic-photonic integration technology, coherent optical communication and DWDM become feasible at high volume. Although currently the main application of electronic-photonic integration technology is long-reach optical communications, its application at shorter-reach promises to overcome the bandwidth limitations of electrical links in the future.

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<td>8:15 AM</td>
<td>Introduction</td>
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<td></td>
<td>Thomas Toifl, Cisco Systems, Zurich, Switzerland</td>
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<td>8:20 AM</td>
<td>Ethernet's Optical Expansion</td>
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<td>John D'Ambrosia, Futurewei, Plano, TX</td>
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<td>9:05 AM</td>
<td>Future Signaling and Coding: Channel Limitations and Potential Solutions above 112G</td>
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<td>Amin Shokrollahi, Kandou Bus and EPFL, Lausanne, Switzerland</td>
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<td>9:50 AM</td>
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<td>Advanced Transceiver Design for 112Gb/s and Beyond</td>
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<td>Electrical Interfaces</td>
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<td>Ronan Casey, Xilinx, Cork, Ireland</td>
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<td>7nm FinFET DSP-Based High-Speed Low-Power Transceiver Design</td>
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<td>11:30 AM</td>
<td>Recent Advancement in Silicon Photonics Foundry</td>
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<td>Luo XianShu, Advanced Micro Foundry (AMF), Singapore</td>
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<td>12:15 PM</td>
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<td>Integrated Silicon Photonics Components for High-Speed Transceivers</td>
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<td>Yuliya Akulova, Intel, Santa Clara, CA</td>
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<td>Advanced Optical Coherent Transceivers Based on Electronic-Photonic Integration Technology</td>
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<td>Takashi Saida, NTT, Kanagawa, Japan</td>
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<td>Monolithic Silicon-Photonic Platforms in CMOS SOI Processes</td>
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<td>Vladimir Stojanovic, Ayar Labs, CA</td>
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This forum will explore a number of trends, topologies, and technologies in support of high-density and fully-integrated power management. System-level strategies for power integration will be explored, such as fine-grained dynamic voltage and frequency scaling and envelope tracking. New architectures for power conversion will be discussed, based on hybrid-resonant switched capacitor topologies as well as high conversion-ratio multiphase converters for performance computing. The forum will also provide an overview of key limitations such as packaging and heat dissipation in high-density power electronics and next generation integrated circuit passive components including silicon-integrated magnets.

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<td></td>
<td>Jason Stauth, Dartmouth College, Hanover, NH</td>
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<td>8:20 AM</td>
<td>System-Level Power Management Strategies for Integrated Platforms</td>
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<tr>
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<td>Vivek De, Intel, Hillsboro, OR</td>
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<tr>
<td>9:05 AM</td>
<td>Next-Generation Circuit Architectures for Power-Supply on Chip</td>
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<tr>
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<td>Hanh-Phuc Le, University of California, San Diego, CA</td>
</tr>
<tr>
<td>9:50 AM</td>
<td>Break</td>
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<tr>
<td>10:00 AM</td>
<td>Distributed Networks of Ultra-Fast Microregulators for Large Scale SoC</td>
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<tr>
<td></td>
<td>Zeynep Toprak-Deniz, IBM, Yorktown Heights, NY</td>
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<tr>
<td>10:45 AM</td>
<td>Advanced Supply Modulator Architectures for Envelope Tracking</td>
</tr>
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<td></td>
<td>in 5G Mobile Handset</td>
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<td></td>
<td>Dongsu Kim, Samsung Electronics, South Korea</td>
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<tr>
<td>11:30 AM</td>
<td>Monolithic Multi-Phase Converters for Medium to High-CURRENT Application Processors</td>
</tr>
<tr>
<td></td>
<td>Juha Pennanen, Texas Instruments, Oulu, Finland</td>
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<tr>
<td>12:15 PM</td>
<td>Lunch</td>
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<tr>
<td>1:30 PM</td>
<td>Integrated Passive Components for Power Supply in Package and Power Supply on Chip - Technology Capabilities and Applications</td>
</tr>
<tr>
<td></td>
<td>Cian Ó Mathúna, Tyndall National Institute, University College Cork, Ireland</td>
</tr>
<tr>
<td>2:15 PM</td>
<td>Packaging Techniques for High Power Density Converter Applications</td>
</tr>
<tr>
<td></td>
<td>Jayden Kim, HANA Micron, Korea</td>
</tr>
<tr>
<td>3:00 PM</td>
<td>Break</td>
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<tr>
<td>3:15 PM</td>
<td>Future Power Passive Components: Chip-Scale Magnetics and High-Q Resonant Structures</td>
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<tr>
<td></td>
<td>Charles R. Sullivan, Dartmouth College, Hanover, NH</td>
</tr>
<tr>
<td>4:00 PM</td>
<td>Conclusion</td>
</tr>
</tbody>
</table>
The forum will discuss application challenges, state-of-the-art and future solutions for health sensing. The talks span the full range from sensor components to applications showing how integrated circuits play a crucial role. Fundamental sensor components, implantable devices, flexible/wearable technology, and advanced circuit design techniques specifically tailored for health sensing will be addressed. Furthermore there will be a clear view on the various emerging sensing techniques and application domains in the health space such as SPAD devices and THz sensing, and how the needs in those domains create opportunities for innovation in ASIC design.

**Agenda**

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td>Breakfast</td>
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<tr>
<td>8:15 AM</td>
<td>Introduction</td>
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<tr>
<td></td>
<td>Matteo Perenzoni, FBK, Trento, Italy</td>
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<tr>
<td>8:20 AM</td>
<td>The Opportunities and Challenges of Silicon ICs in Biosensing Platforms:</td>
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<td></td>
<td>From mm-Scale Multiplexed Bio-molecular Sensors to Cell-based Assays</td>
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<td>Kaushik Sengupta, Princeton University, Princeton, NJ</td>
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<tr>
<td>9:05 AM</td>
<td>Implantable Wireless Microdevices for Recording Neural Activity</td>
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<td>in Brain Circuits</td>
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<td>Arto Nurmikko, Brown University, Providence, RI</td>
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<tr>
<td>9:50 AM</td>
<td>Break</td>
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<tr>
<td>10:00 AM</td>
<td>Conformal Thin-Film Electronics</td>
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<tr>
<td></td>
<td>Takao Someya, University of Tokyo, Tokyo, Japan</td>
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<tr>
<td>10:45 AM</td>
<td>Flexible Electronics for Medical Imaging:</td>
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<td></td>
<td>from Patches to Large-Area X-Ray Imaging</td>
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<tr>
<td></td>
<td>Kris Myny, IMEC, Leuven, Belgium</td>
</tr>
<tr>
<td>11:30 AM</td>
<td>SPADs, ISFETs and Photodiodes: Mixed-Mode Sensing for Healthcare</td>
</tr>
<tr>
<td></td>
<td>David Cumming, University of Glasgow, Glasgow, United Kingdom</td>
</tr>
<tr>
<td>12:15 PM</td>
<td>Lunch</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>CMOS Sensor Architectures and Circuital Solutions for Nuclear Medicine:</td>
</tr>
<tr>
<td></td>
<td>from Scintillator-Based dSiPM to Monolithic Detectors</td>
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<tr>
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<td>Nicola Massari, FBK, Trento, Italy</td>
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<tr>
<td>2:15 PM</td>
<td>CMOS/BiCMOS THz System-on-Chip for Life-Science Applications</td>
</tr>
<tr>
<td></td>
<td>Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany</td>
</tr>
<tr>
<td>3:00 PM</td>
<td>Break</td>
</tr>
<tr>
<td>3:15 PM</td>
<td>Circuit Design for Ultrasound on a Chip (Short demo at the end of presentation)</td>
</tr>
<tr>
<td></td>
<td>Kailiang Chen, Butterfly Network, Guilford, CT</td>
</tr>
<tr>
<td>4:00 PM</td>
<td>Conclusion</td>
</tr>
</tbody>
</table>
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<td>6:30 am to 3:00 pm</td>
<td>8:00 am to 3:00 pm</td>
<td>8:00 am to 3:00 pm</td>
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</table>

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST Sunday January 12, 2020. After January 12th, and before 12:00 Midnight EST Sunday January 26, 2020, registrations will be processed at the Late Registration rates. After January 26th, you must register at the on-site rates. You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 12:00 Midnight EST Sunday January 26, 2020, conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. No refunds will be made after 12:00 Midnight EST January 26, 2020. Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with WRITTEN permission from the original registrant.

IEEE Membership Saves on ISSCC Registration
Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you’re an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/about/help/member_support.html. If you’re not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you’ll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

SSCS Membership – a Valuable Professional Resource for your Career Growth
Get Connected! Stay Current! Invest in your Career! Membership in the Solid-State Circuits Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

SSCS Membership delivers:
- Networking with peers
- Educational development
- Tools for career growth
- Leadership opportunities
- Recognition for your achievements
We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuits Society where you can:

- Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.
- Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine “Solid-State Circuits Magazine”, and our award winning “Journal of Solid-State Circuits”.
- Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.
- Access publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world’s technical research to keep your knowledge current. Publications included in your SSCS membership are the “RFIC Virtual Journal” (RFVJ) and the “Journal on Exploratory Solid-State Computational Devices and Circuits” (JxCDC), Solid-State Letters, and our newest Journal, the “Open Journal of Solid State Circuits” (OJ-SSC) an open access publication.

SSCS Membership Saves Even More on ISSCC Registration
This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE’s Solid-State Circuits Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day’s papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Universal Travel Adapter: A compact travel power adapter will be given to all Conference registrants.

Publications: Conference registration includes:
- The Digest of Technical Papers on USB. This year, as part of your Conference registration, the e-Digest of Technical Papers will be provided on a USB, as well as part of the download. The e-Digest will include all 3 pages for each paper. Also, the print Digest will be available at a cost of $75, but does not include the 3rd page (additional figures and references). Note that all 3 pages for each paper will be available on IEEE Xplore.
- Papers Visuals: The visuals from all papers presented will be available by download.
- Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be available by download.

Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.
OPTIONAL EVENTS
Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times. A “Thursday All-Access Pass” is available that provides access to all Thursday educational events and a copy of each course handout. Pick just the speakers you want to hear!

OPTIONAL PUBLICATIONS
ISSCC 2020 Publications: The following ISSCC 2020 publications can be purchased in advance or on site:
- 2020 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) (mailed in March).
- 2020 Digest of Technical Papers in hard copy.
- 2020 Tutorials USB: All of the 90 minute Tutorials (mailed in June).
- 2020 Short Course USB: Circuit Design in Advanced CMOS Technologies —Considerations and Solutions” (mailed in June).
The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.
Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:
- Items listed on the registration website can be purchased with registration and picked up at the conference.
- Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.
- Visit the ISSCC website at www.isscc.org and click on the link “About/Shop ISSCC/Shop Now” where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS
Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. Conference room rates are $285 for a single/double, $310 for a triple and $335 for a quad (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive in-room Internet access for free. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.
Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for “Reservations.” When making your reservation, identify the group as ISSCC 2020 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 26, 2020 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached or after January 26th, the group rates may no longer be available and reservations will be filled at the best available rate. Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for “Reservations”). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY
IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.
CONFERENCE INFORMATION

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee’s image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video or audio recording by participants or other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website: www.isscc.org
ISSCC Email: ISSCC@ieee.org
Registration questions: ISSCCinfo@yesevents.com
Hotel Information: San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information: Kenneth C. Smith University of Toronto Email: lcfujino@aol.com Phone: 416-418-3034
Registration: YesEvents PO Box 3024 Westminster, MD 21158 Phone: 800-937-8728 Email: issccinfo@yesevents.com Fax: 410-559-2236

Hotel Transportation: Visit the ISSCC website “Registration/Transportation from Airport” page for helpful travel information and links. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2021 will be held on February 14-18, 2021 at the San Francisco Marriott Marquis Hotel.

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